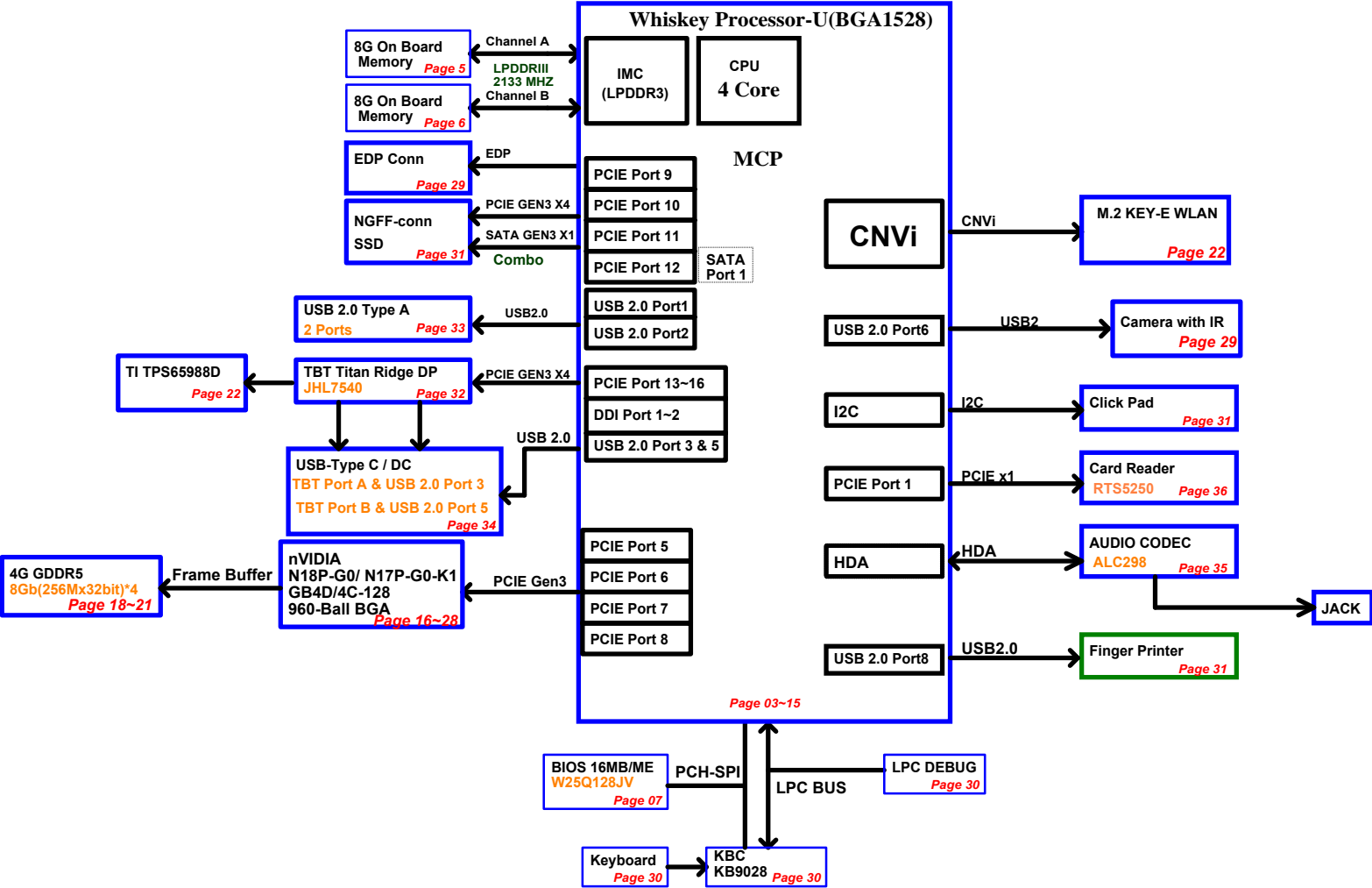


# Whiskey Lake Processor-U Platform MS-14C1 VER : A





SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

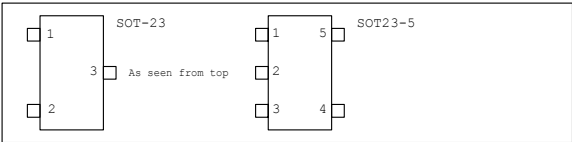
Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_05VSUS	1.0V power rail	+1_8VSUSPWROK
+1_8VSUS	1.8V power rail	3V5VPWROK
+1_2VDIMM/+1_8VDIMM	1.2V power rail DDR (off in S4-S5)	S4_DIMM_ON_AND
+VDDQ_CPU	1.2V power rail CPU DRAM (off in S4-S5)	S4_DIMM_ON_AND
+VCCST/+VCCPLL	1.0V power rail CPU (off in S4-S5)	+1_2VDIMM_PWRGD
+VCCSTG	1.0V power rail CPU (off in S3-S5)	RUND
+5VRUN	5.0V switched power rail (off in S3-S5)	RUND
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUND
+0_6VRUN	0.6V DDR Termination voltage (off in S3-S5)	DDR_VTT_CTRL
+1_8VRUN	1.8V power rail AUDIO (off in S3-S5)	RUND
+VCC_IO	1.0V rail for Processor & PCH (off in S3-S5)	RUND
+VCC_SA	0.55V to 1.15V Voltage for Processor	VR_ON
+VCC_GT	0.55V to 1.52V Core Voltage for Processor	VR_ON
+VCC_CORE	0.55V to 1.5V Voltage for Processor	VR_ON

Net Naming Conventions

Suffix
# = Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALWAYS	+3VSUS	+*VSUS	+*VRUN	+VTT_CORE	Clocks
S0( Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON
S3( Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	ON	OFF	OFF	OFF
S4( Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF	OFF
S3( Suspend to RAM) WOL_EN	LOW	HIGH	HIGH	ON	ON	ON	OFF	OFF	OFF
S4( Suspend to Disk) WOL_EN	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF	OFF
S5 (Soft OFF) WOL_EN	LOW	LOW	LOW	ON	ON	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V\*SUS will always keep high

MICRO-STAR INT'L CO.,LTD.

Title

PLATFORM

Size

Custom

Document Number

MS-14C1

Date:

Wednesday, May 29, 2019

Sheet

2 of 56

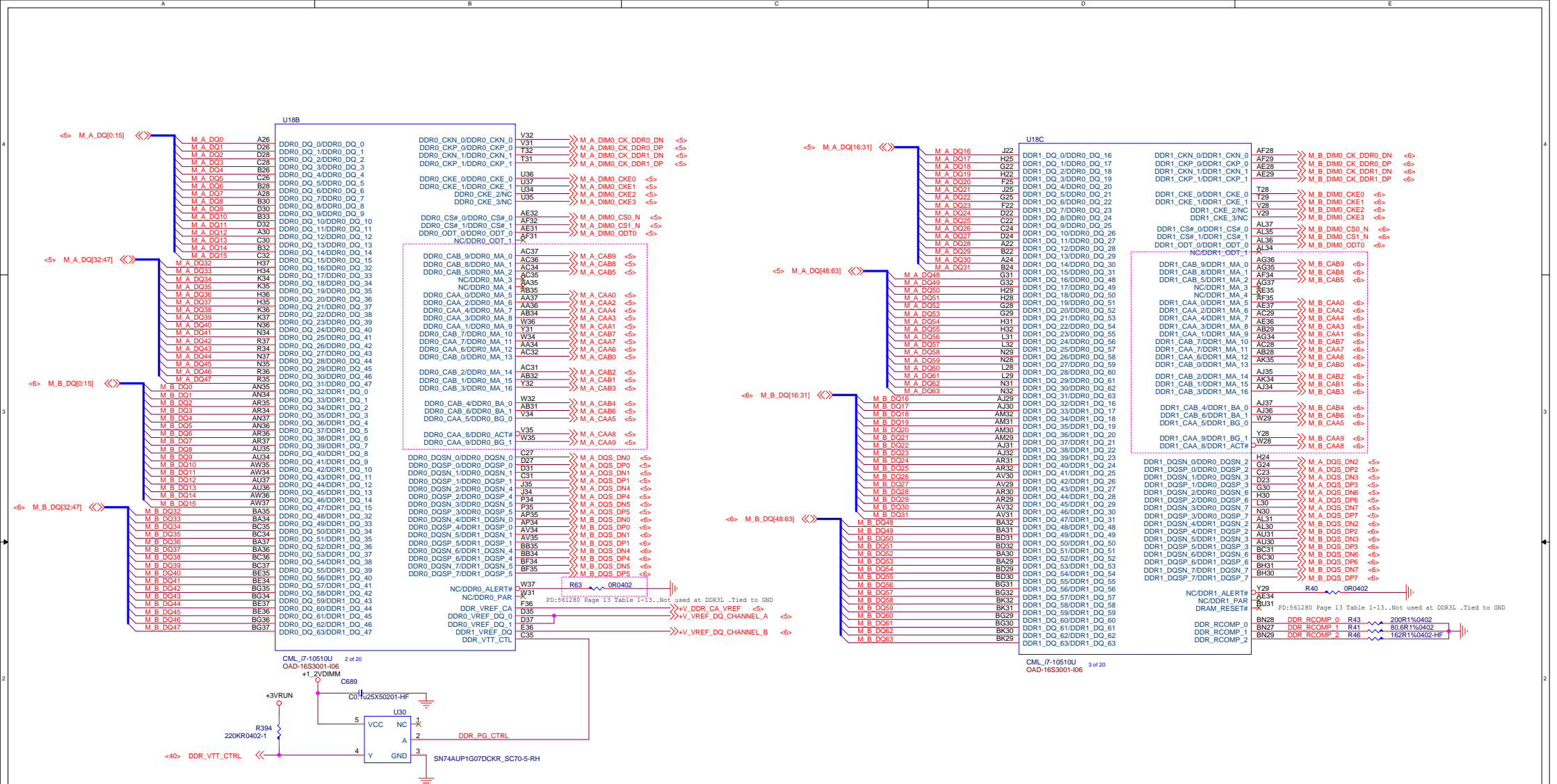
Rev

0A



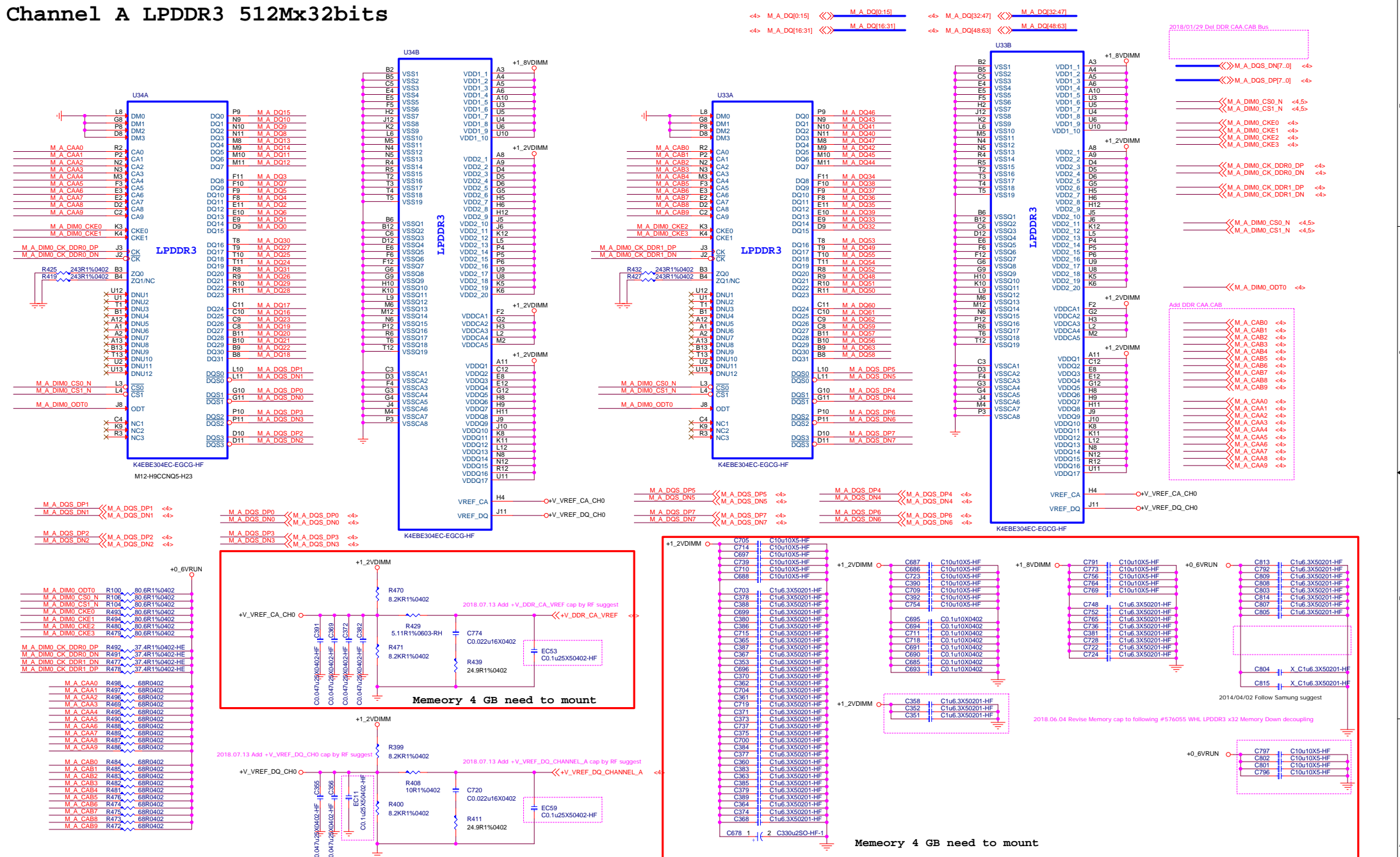






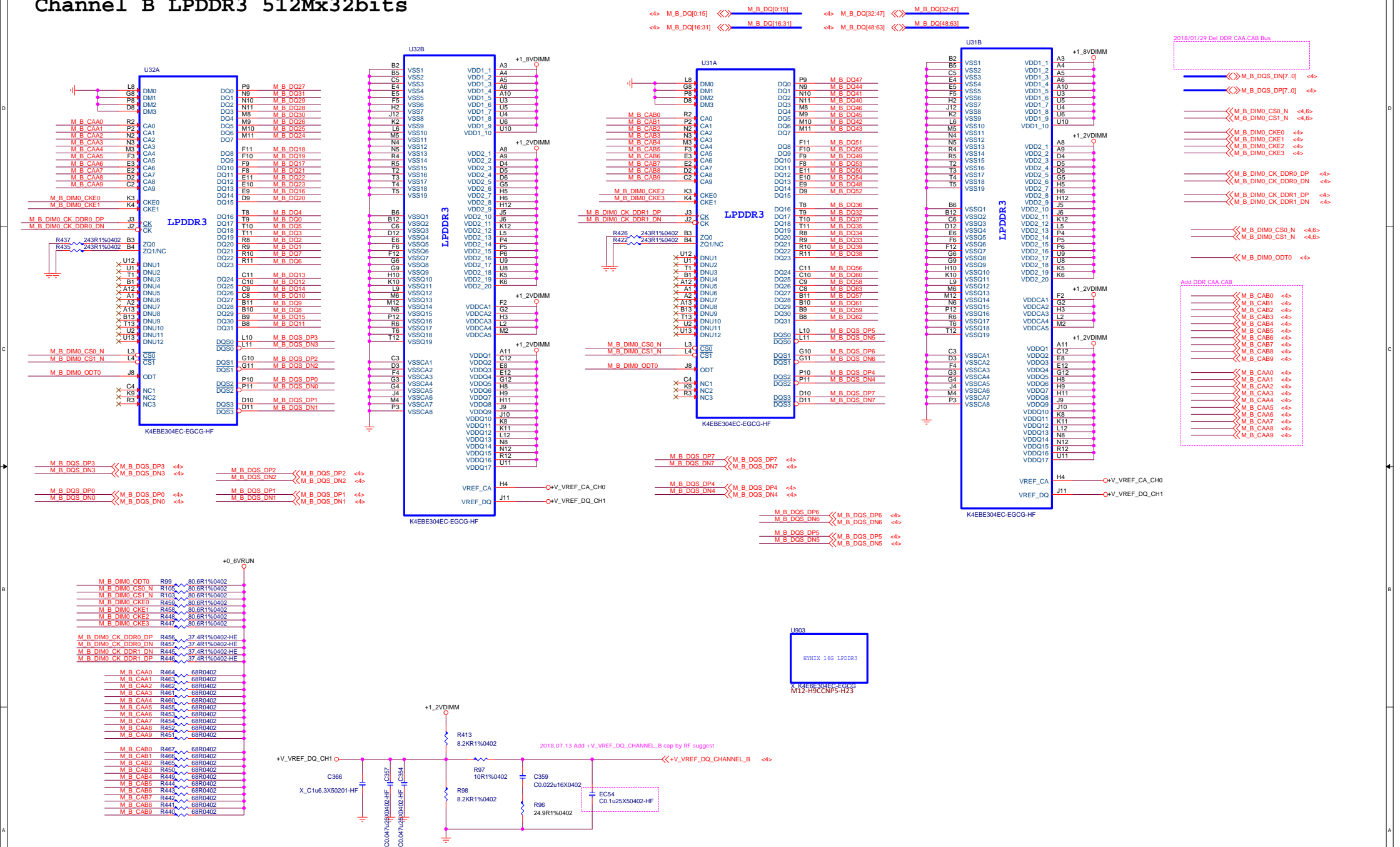


**Channel A LPDDR3 512Mx32bits**





**Channel B LPDDR3 512Mx32bits**





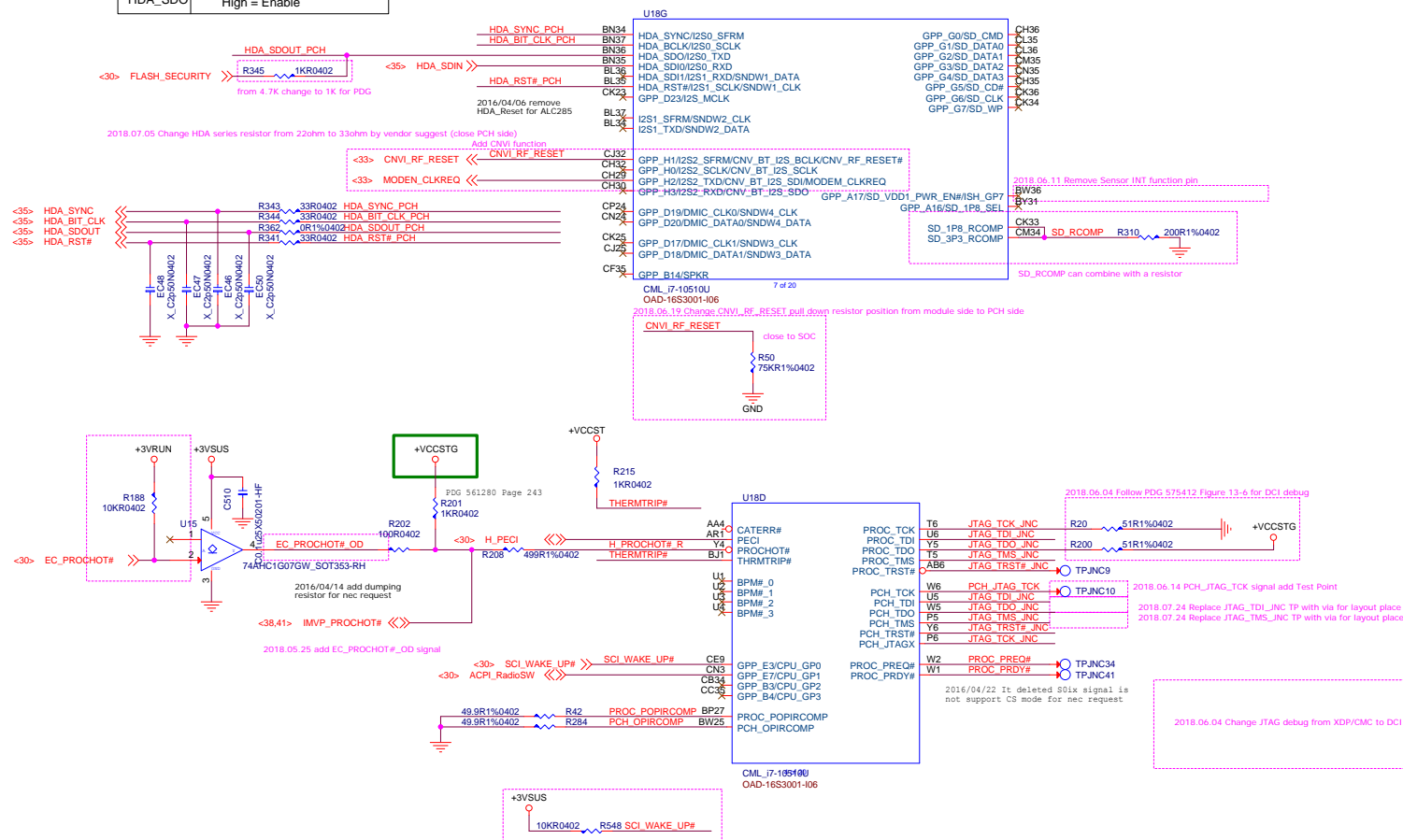




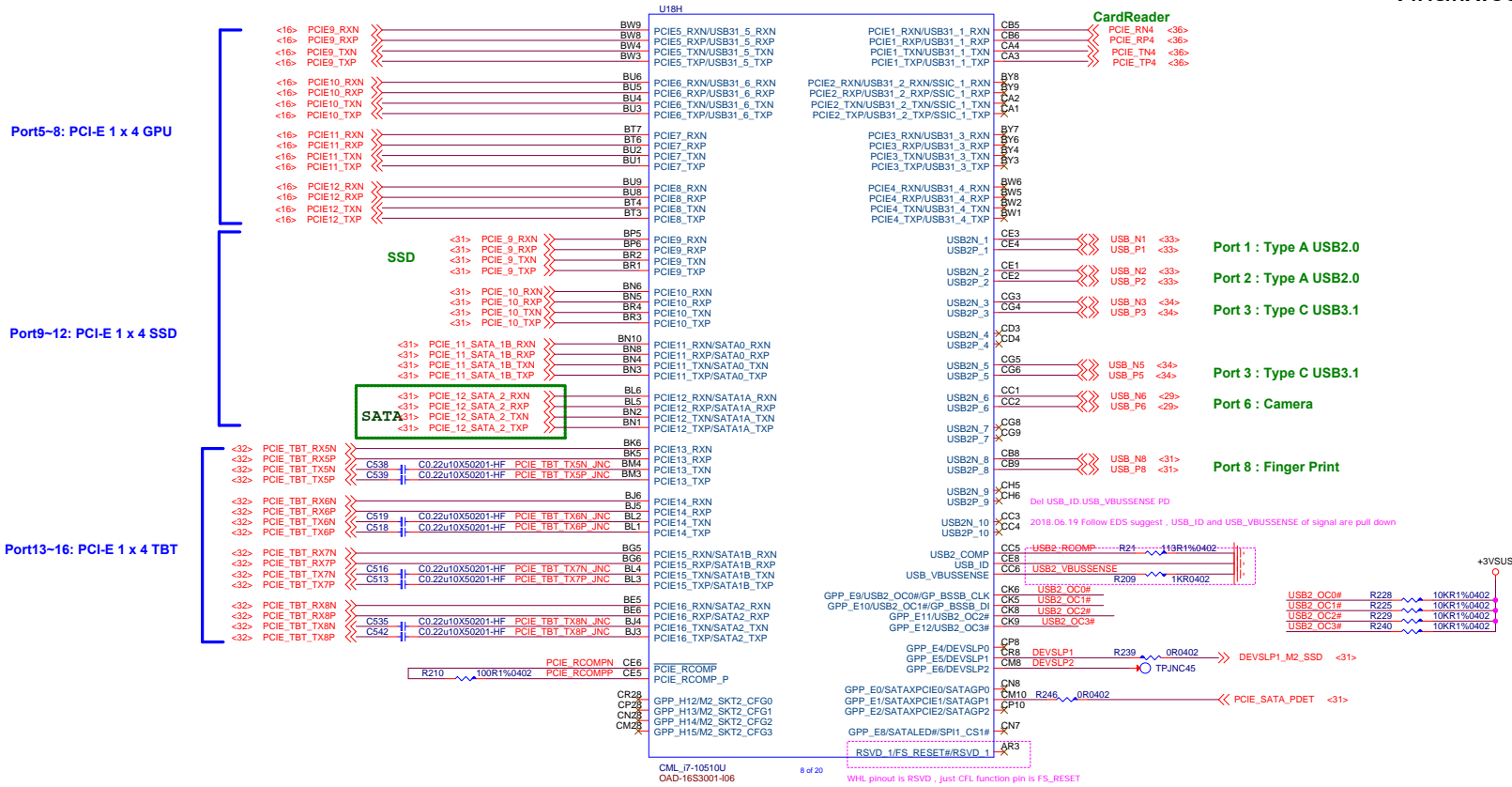
2018.06.01 Revise memory configuration table



Flash Descriptor Security Override	
HDA_SDO	Low = Disable High = Enable



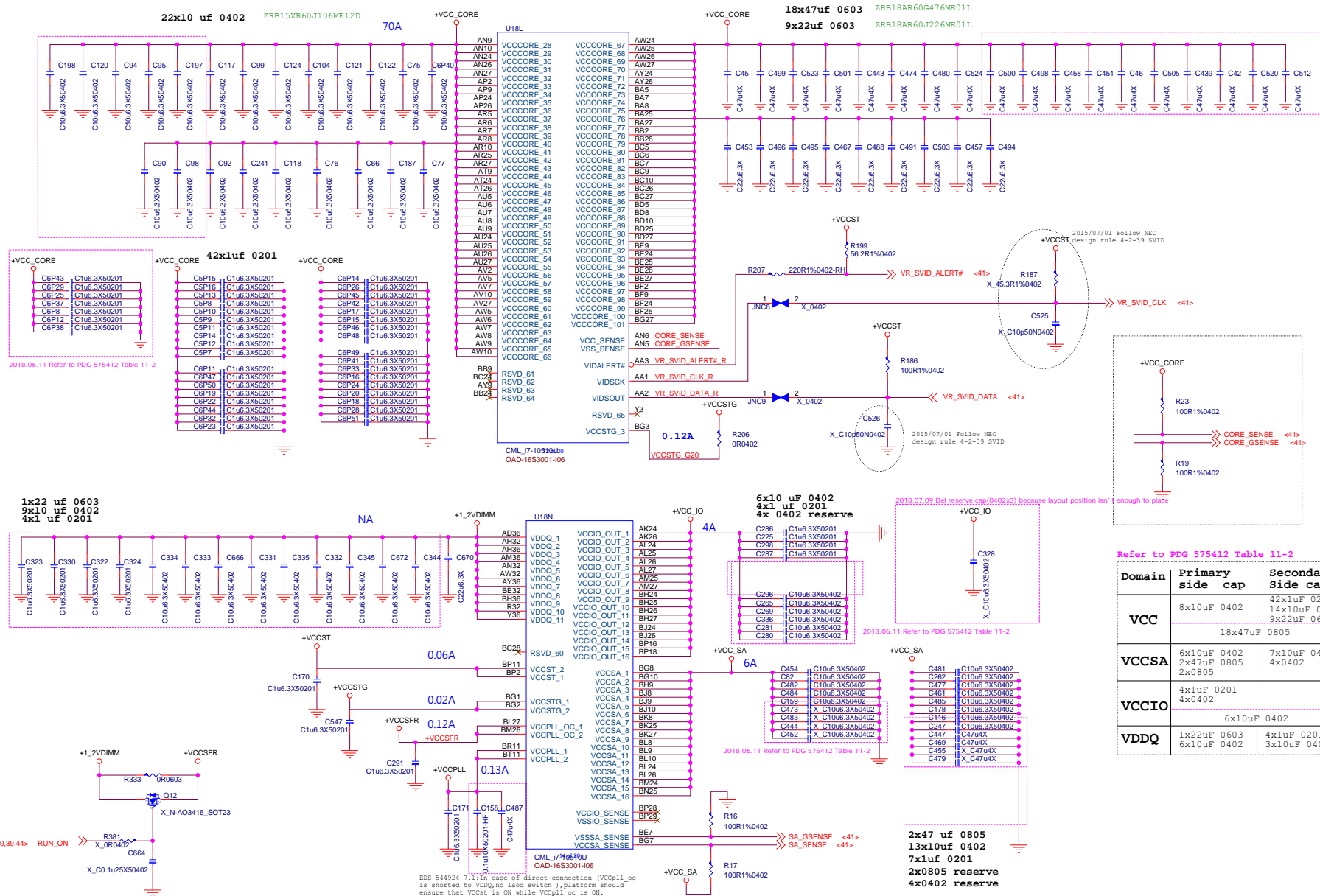




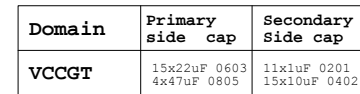












VCCOPC/VCCOPC\_1P8 . VCCEOPIO for U43e only









U18R

CR34	VSS_342	VSS_330	BL7
BT5	VSS_351	VSS_337	AE25
CP35	VSS_361	VSS_345	BM33
CM37	VSS_371	VSS_354	CM5
CK37	VSS_381	VSS_364	AE27
AW11	VSS_391	VSS_374	BM35
CM1	VSS_401	VSS_384	CM9
AE24	VSS_411	VSS_392	P3
BD6	VSS_421	VSS_398	B7
AT4	VSS_431	VSS_402	AE30
B34	VSS_360	VSS_315	BM36
E35	VSS_370	VSS_322	CM13
A4	VSS_380	VSS_329	CM17
AE24	VSS_390	VSS_336	P36
AE26	VSS_400	VSS_344	BA10
AF25	VSS_410	VSS_353	CC11
AG24	VSS_420	VSS_363	P4
AG26	VSS_428	VSS_373	BA28
AH24	VSS_434	VSS_385	P7
B2	VSS_350	VSS_307	BA3
B36	VSS_359	VSS_314	CC20
CP36	VSS_369	VSS_321	R27
C37	VSS_379	VSS_328	BB3
CM1	VSS_389	VSS_335	CC25
CM2	VSS_399	VSS_343	R28
CM37	VSS_409	VSS_352	BB33
CP2	VSS_419	VSS_362	CC28
D1	VSS_427	VSS_369	R29
A32	VSS_435	VSS_375	BB36
F33	VSS_341	VSS_432	CC31
A3	VSS_349	VSS_294	R30
B17	VSS_358	VSS_300	BB4
C136	VSS_368	VSS_306	CC7
A36	VSS_378	VSS_313	R31
BK10	VSS_388	VSS_320	CC25
C14	VSS_398	VSS_327	CD11
AB27	VSS_408	VSS_334	T27
BK2	VSS_418	VSS_340	CD12
CK1	VSS_428	VSS_345	T30
AB3	VSS_333	VSS_424	BC29
BK28	VSS_340	VSS_431	CD14
AB30	VSS_348	VSS_293	T33
BK3	VSS_357	VSS_299	T35
CK4	VSS_367	VSS_305	BC32
AB33	VSS_377	VSS_312	CD24
BK33	VSS_387	VSS_319	T36
CK7	VSS_397	VSS_326	CD25
AB36	VSS_407	VSS_334	T7
BK4	VSS_417	VSS_340	BC8
CL2	VSS_325	VSS_414	CE33
AB4	VSS_332	VSS_423	U26
BK7	VSS_339	VSS_430	BD28
CM13	VSS_347	VSS_292	CE35
AB7	VSS_356	VSS_298	U7
BL25	VSS_366	VSS_304	BD33
CM17	VSS_376	VSS_311	CE36
AC10	VSS_386	VSS_318	V26
BL28	VSS_396	VSS_323	BD35
CM21	VSS_406	VSS_328	CE7
AC27	VSS_317	VSS_403	V27
BL29	VSS_324	VSS_413	BD36
CM25	VSS_331	VSS_422	CF11
AC30	VSS_346	VSS_291	V3
BL30	VSS_355	VSS_297	BE10
CM29	VSS_365	VSS_303	CF14
BL31	VSS_375	VSS_310	BE28
AD33	VSS_385	VSS_317	CF19
BL32	VSS_395	VSS_322	V33
CM33	VSS_405	VSS_327	BE29
VSS_316	VSS_402	AL29	CF2
VSS_323	VSS_412		V36
			BE3

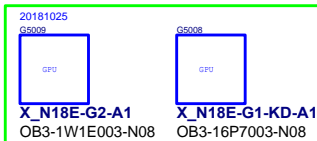
CM14 0510U  
OAD-16S3001-106

U18T

N6	VSS_96	VSS_90	CF23
B37	VSS_73	VSS_106	V4
CB3	VSS_79	VSS_115	W10
P10	VSS_84	VSS_126	BE30
B5	VSS_89	VSS_130	W28
CB33	VSS_95	VSS_8	BE31
P3	VSS_102	VSS_19	W33
B7	VSS_110	VSS_29	W27
CB4	VSS_120	VSS_43	CF3
P33	VSS_132	VSS_87	BF4
B9	VSS_145	VSS_92	W30
CB7	VSS_14	VSS_98	CF33
P36	VSS_25	VSS_105	W7
BA10	VSS_35	VSS_114	BE33
CC11	VSS_44	VSS_125	CG7
P4	VSS_52	VSS_138	W26
BA28	VSS_59	VSS_500	BF4
P7	VSS_65	VSS_18	W37
BA3	VSS_72	VSS_77	CG25
CC20	R27	VSS_82	CG26
R27	VSS_131	VSS_86	CJ11
BB3	VSS_144	VSS_91	Y33
CC25	R28	VSS_97	CJ14
R28	VSS_13	VSS_104	Y35
BB33	VSS_24	VSS_113	BE128
CC28	VSS_34	VSS_124	BE129
R29	VSS_51	VSS_137	BE130
BB36	VSS_58	VSS_6	BE131
CC31	R30	VSS_70	BE132
R30	BB4	VSS_76	BE133
BB4	CC7	VSS_119	BE134
CC7	R31	VSS_130	BE135
R31	CC25	VSS_143	BE136
CC25	CD11	VSS_12	BE137
CD11	T27	VSS_23	BE138
T27	CD12	VSS_33	BE139
CD12	T30	VSS_42	BE140
T30	BC29	VSS_50	BE141
BC29	CD14	VSS_57	BE142
CD14	T33	VSS_63	BE143
T33	T35	VSS_69	BE144
T35	BC32	VSS_109	BE145
BC32	CD24	VSS_118	BE146
CD24	T36	VSS_129	BE147
T36	CD25	VSS_142	BE148
CD25	T7	VSS_22	BE149
T7	CE8	VSS_32	BE150
CE8	BC38	VSS_41	BE151
BC38	U26	VSS_49	BE152
U26	BD28	VSS_56	BE153
BD28	CE35	VSS_101	BE154
CE35	U7	VSS_108	BE155
U7	BD33	VSS_117	BE156
BD33	CE36	VSS_128	BE157
CE36	V26	VSS_141	BE158
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BD36	CF11	VSS_48	BE163
CF11	V3	VSS_94	BE164
V3	BE10	VSS_99	BE165
BE10	CF14	VSS_107	BE166
CF14	V30	VSS_116	BE167
V30	BE28	VSS_127	BE168
BE28	CF19	VSS_140	BE169
CF19	V33	VSS_150	BE170
V33	BE29	VSS_159	BE171
BE29	CF2	VSS_168	BE172
CF2	V36	VSS_177	BE173
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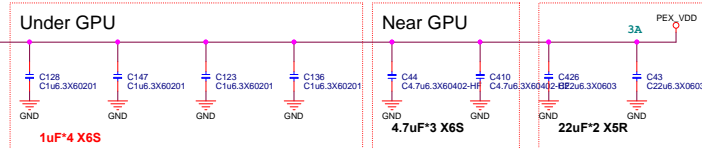


# GPU PCI EXPRESS

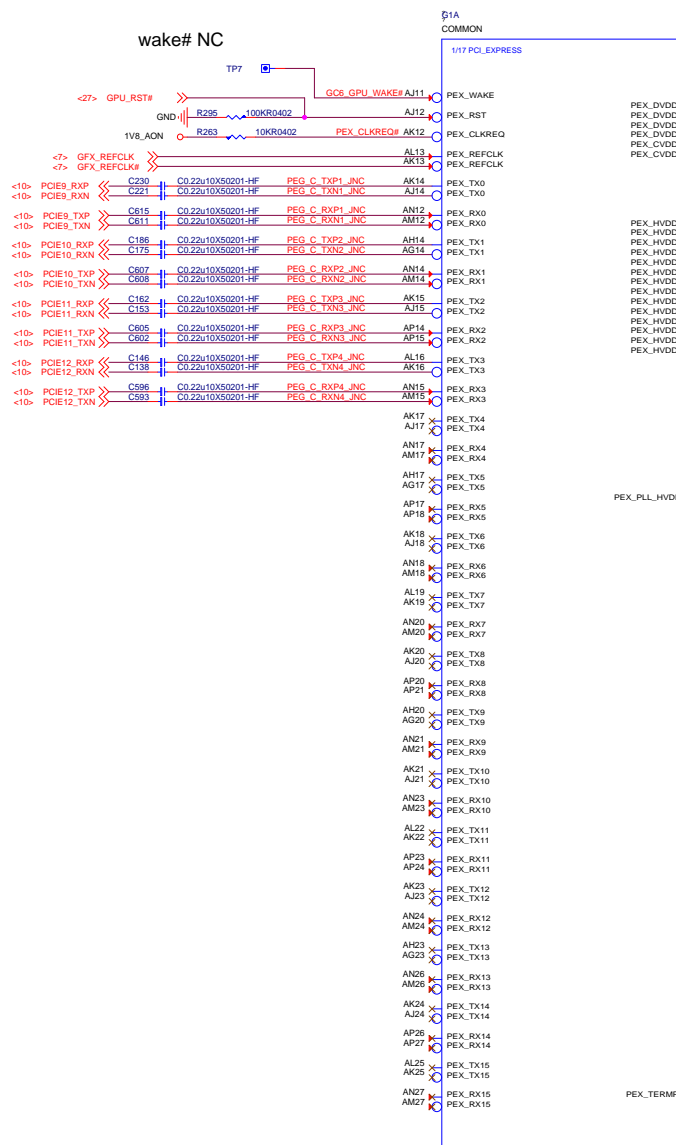


N18:0.47u\*15,change 10,4.7u\*3,10u\*3,22u\*2  
N17:1u\*4,4.7u\*2,10u,22u\*1

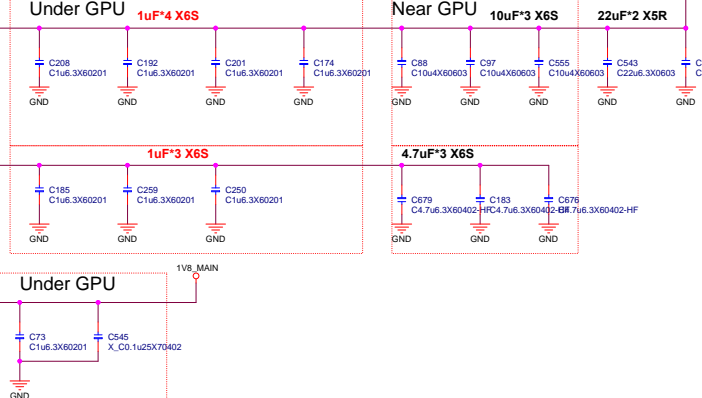
N18 :1u\*6



PEX_DVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5R
N17P	4	2	1	1
N18P	6	3	3	2



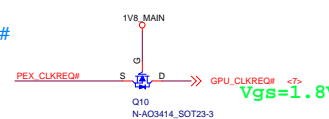
N18 :1u\*7



PEX_HVDD	1uF X6S	4.7uF X6S	10uF X6S	22uF X5R
N17P	4	2	2	1
N18P	7	3	3	2

Vinafix.com

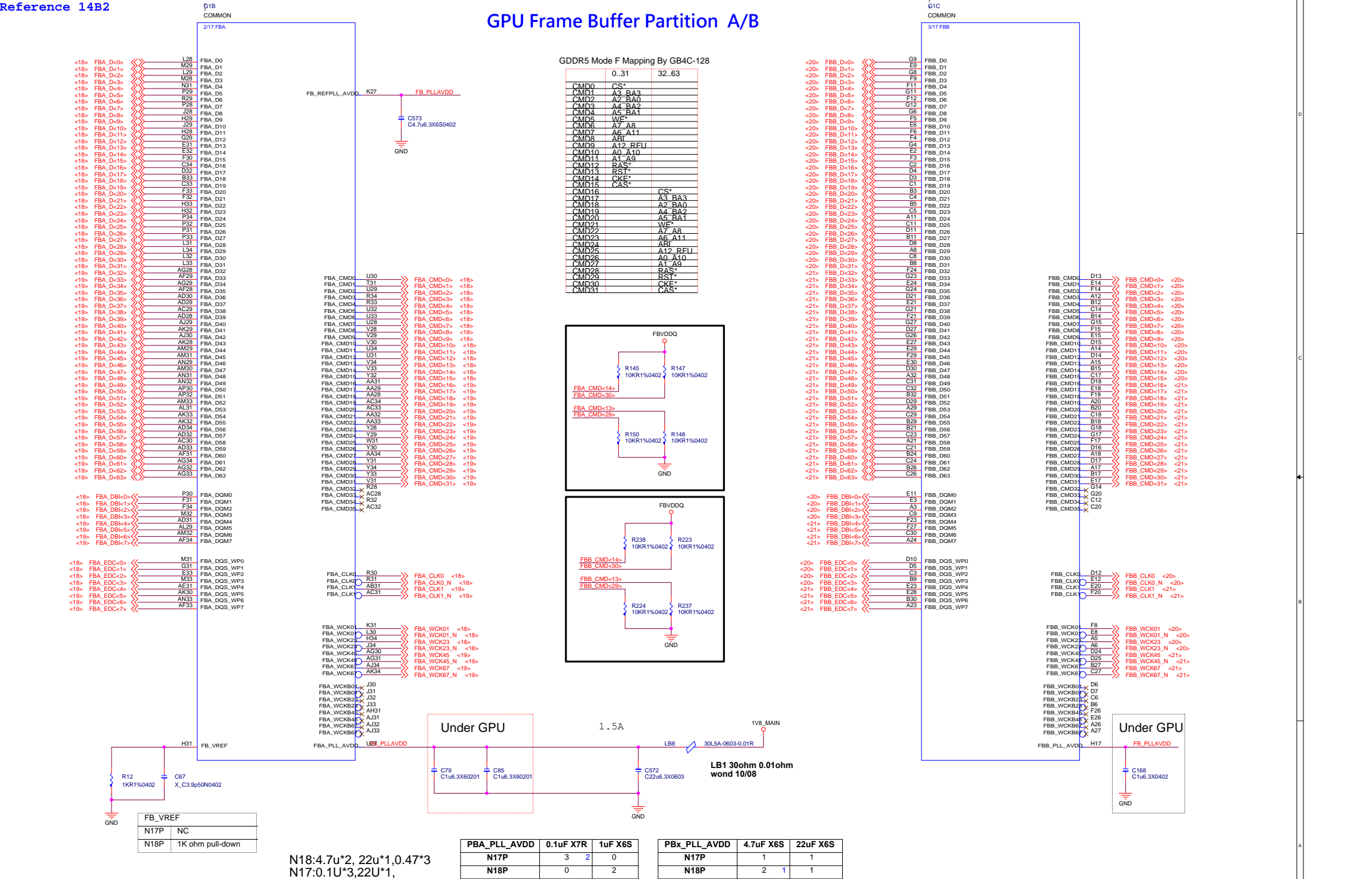
GPU CLK REQ#



Vgs=1.8V

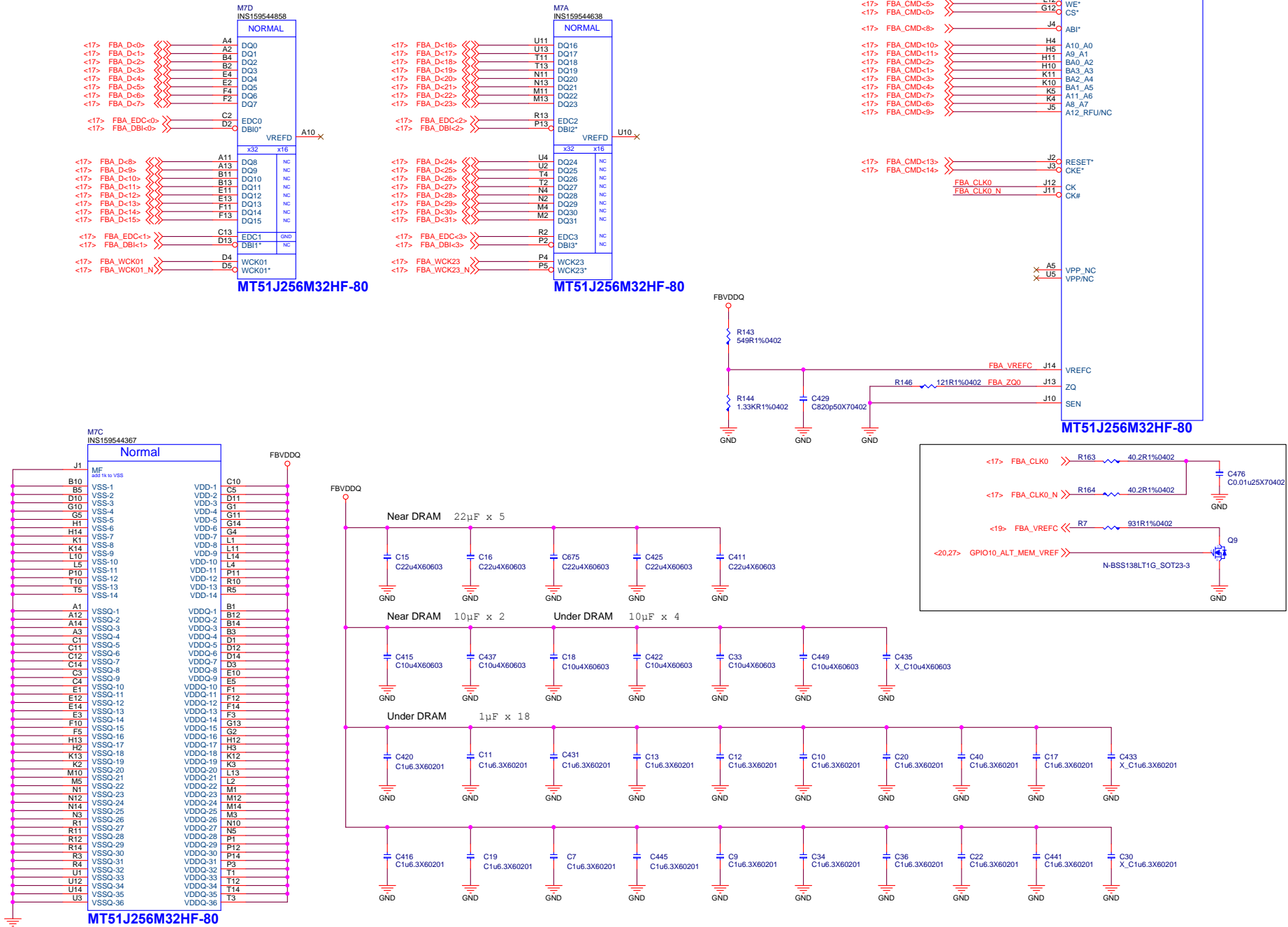


GPU Frame Buffer Partition A/B



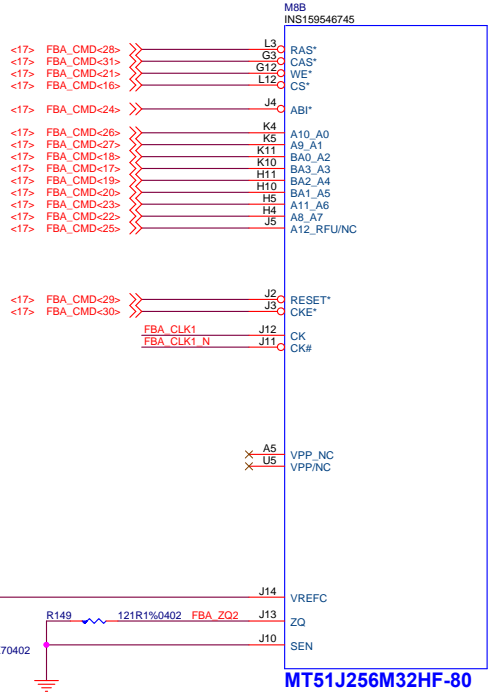
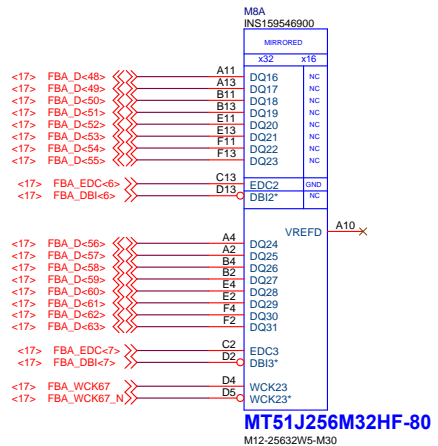
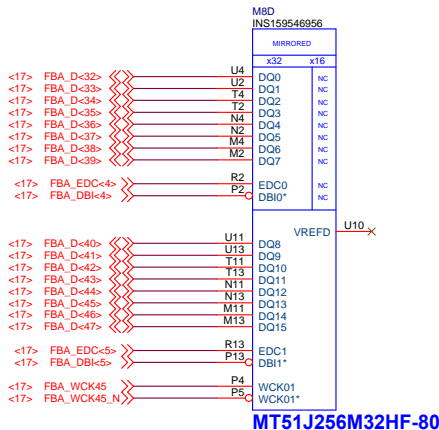


# DGPU\_GDDR5 FrameBuffer A0



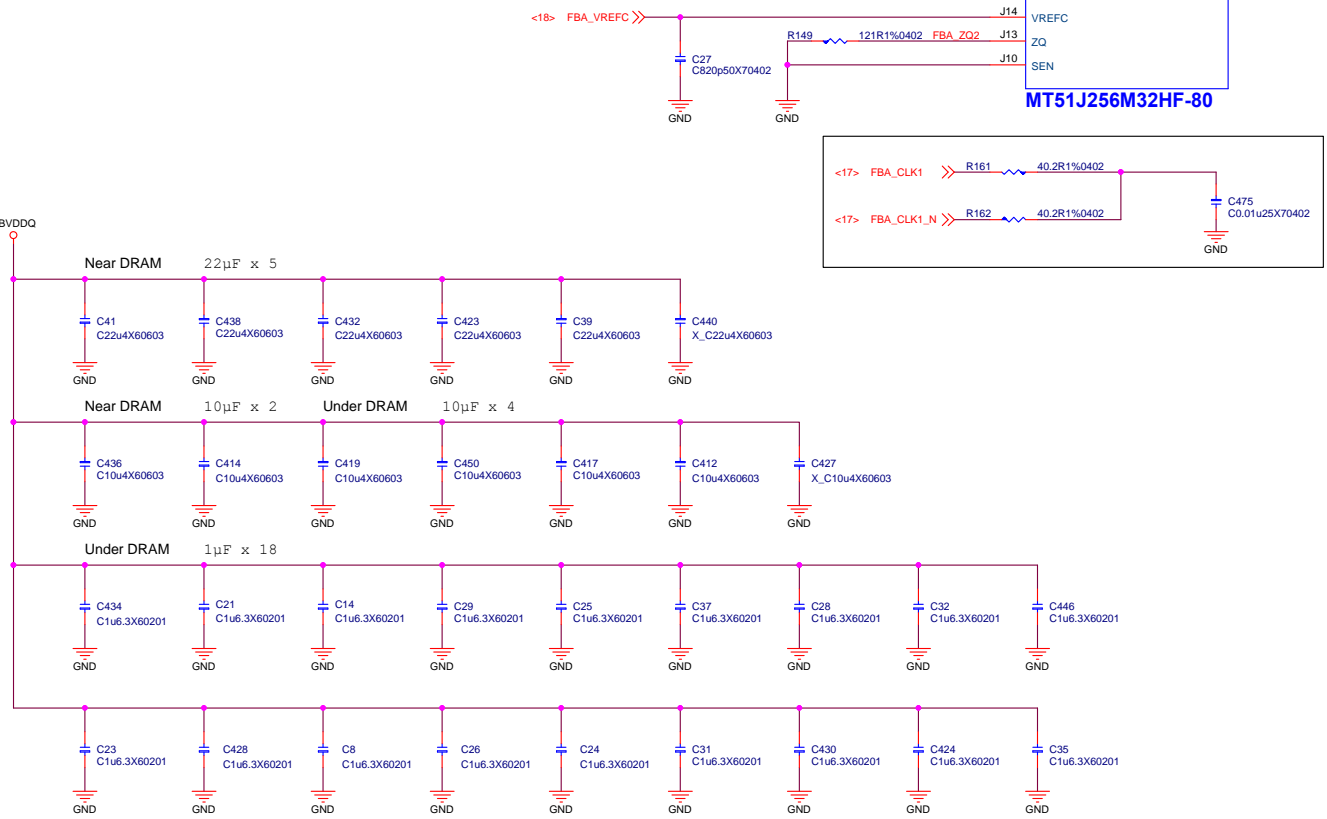
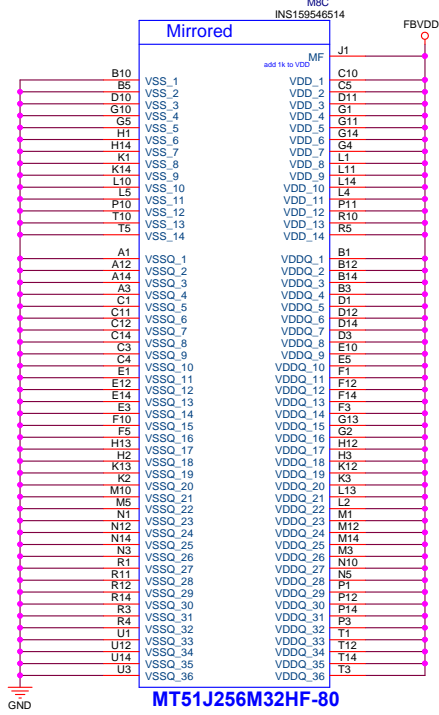


DGPU\_GDDR5 FrameBuffer A1



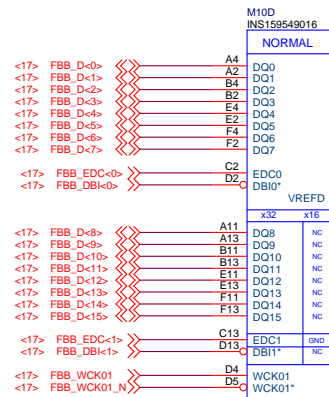
Vinafix.com

2016/03/23 Remove R14 to follow NV CRB

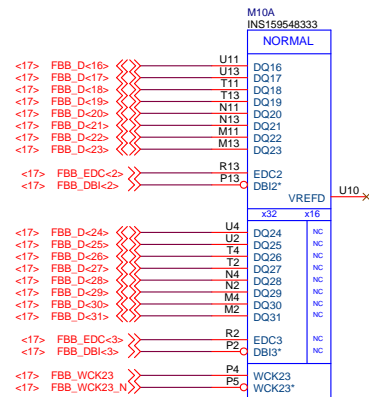




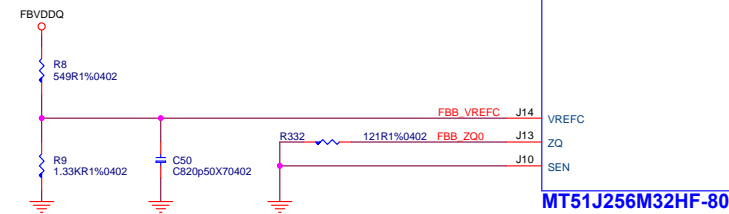
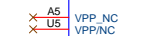
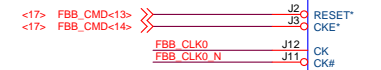
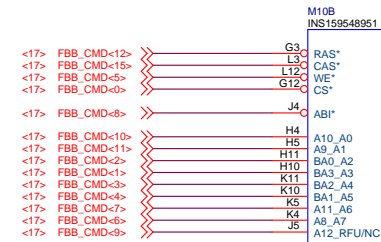
## DGPU\_GDDR5 FrameBuffer B0



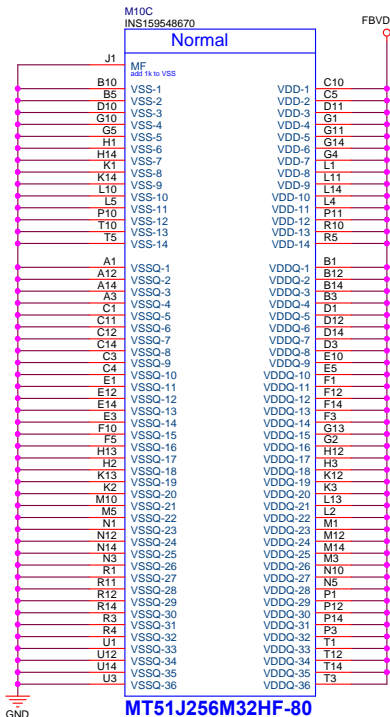
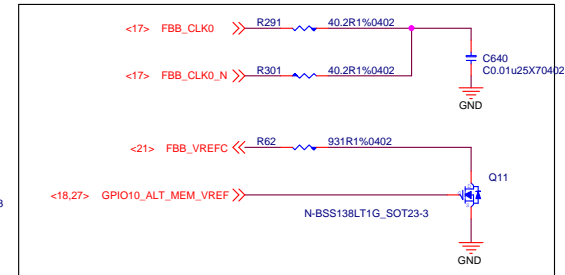
MT51J256M32HF-80



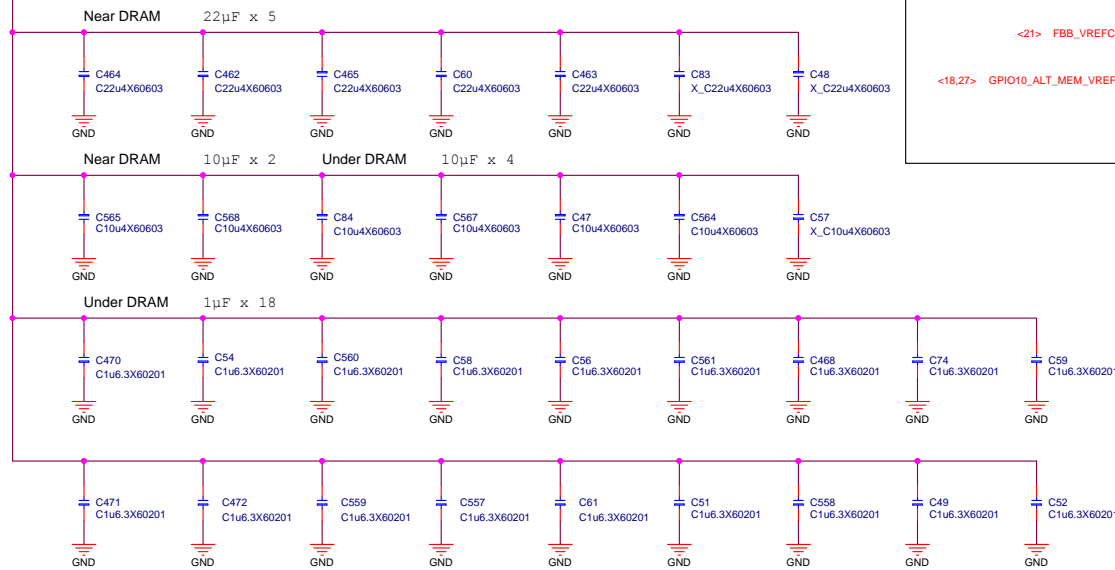
MT51J256M32HF-80



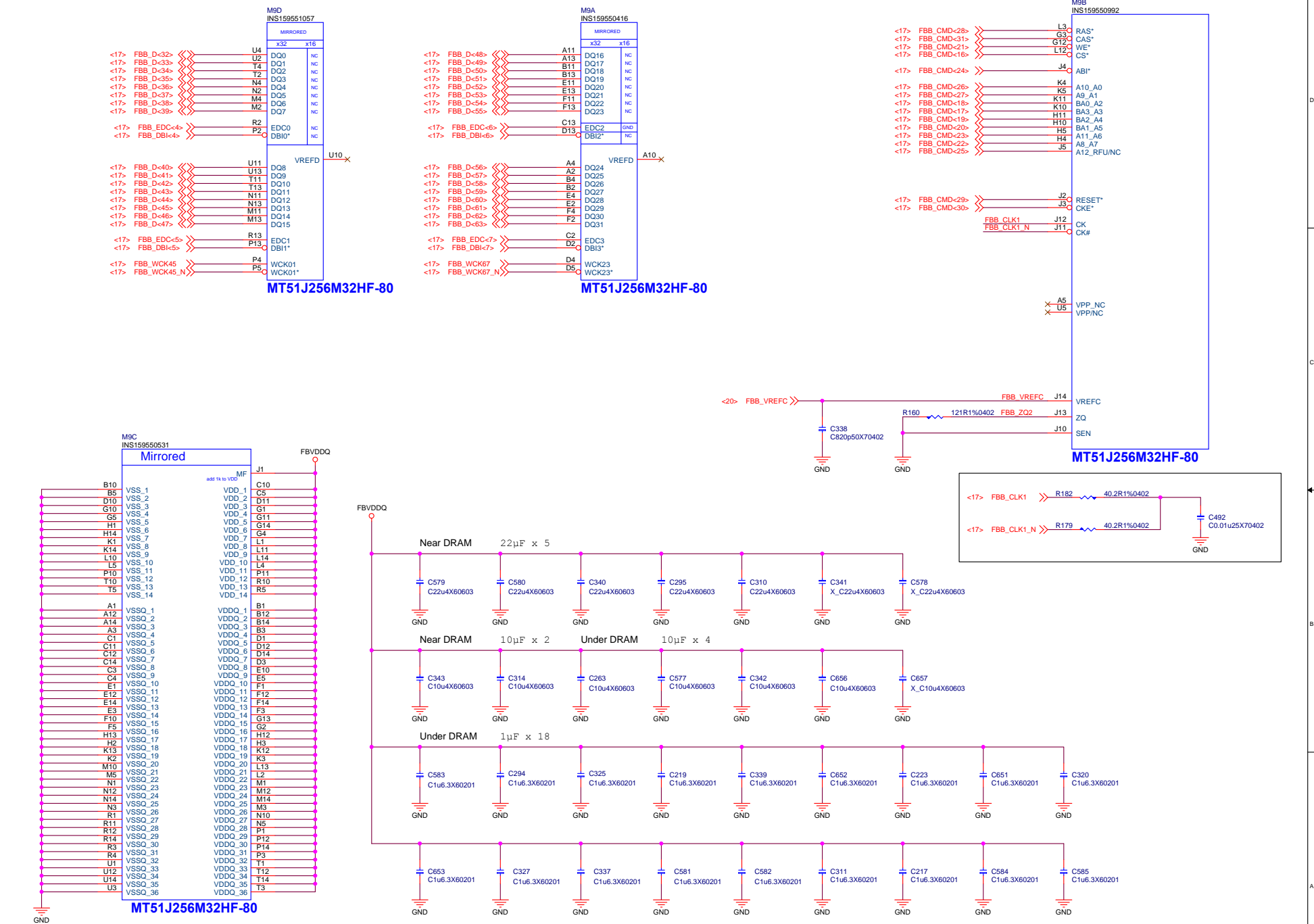
MT51J256M32HF-80



**MT51J256M32HF-80**

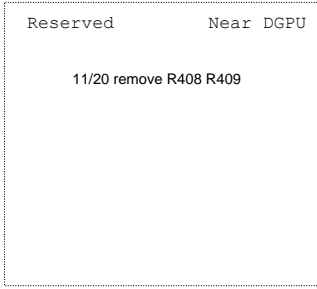
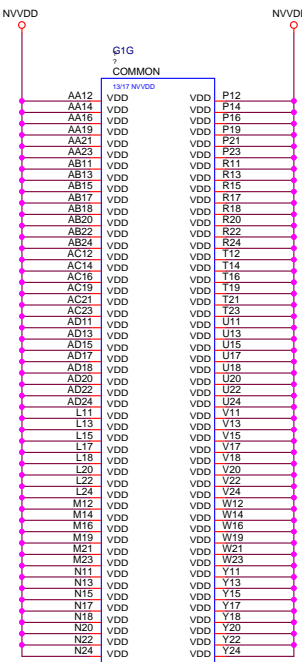




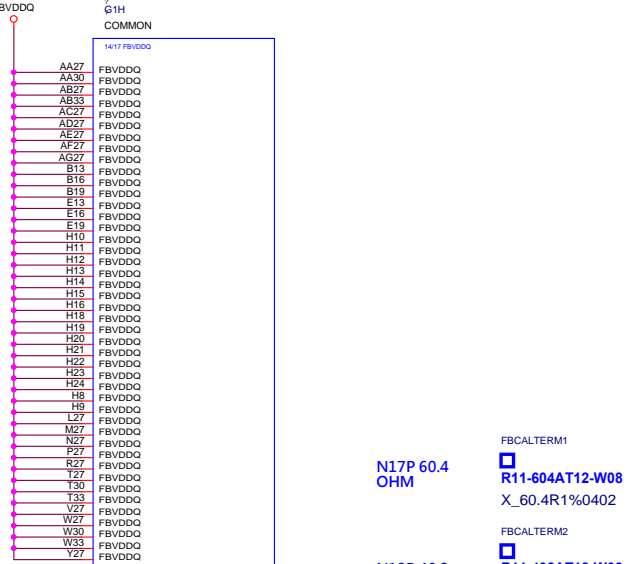
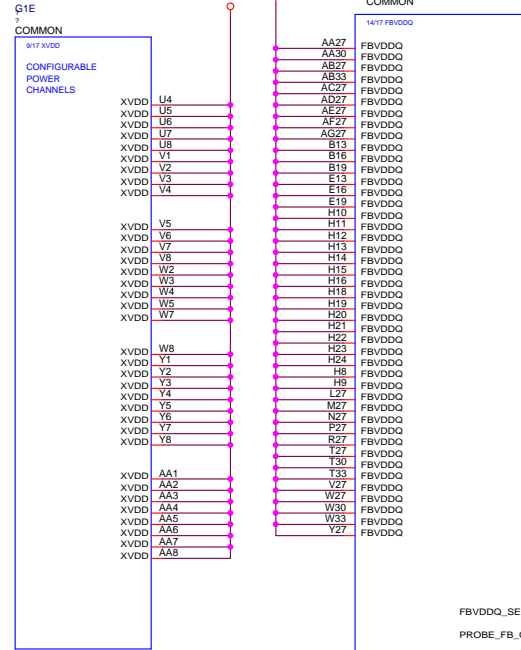
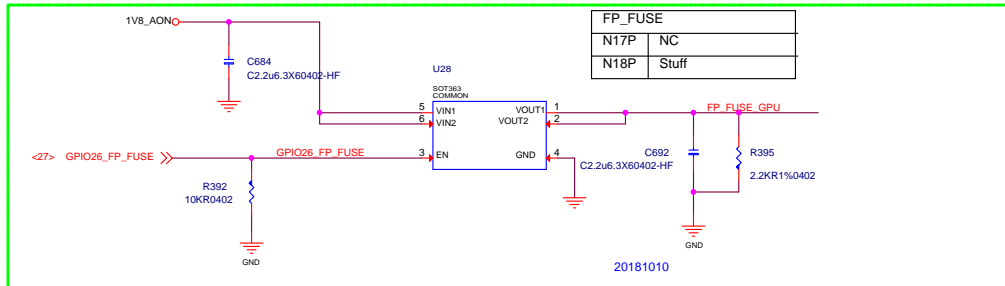
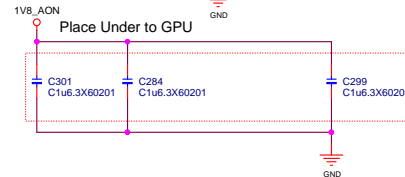
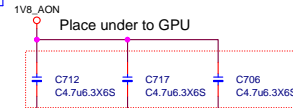
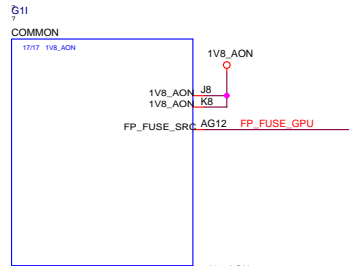




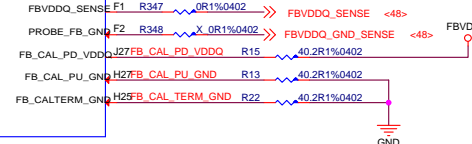
# GPU NVVDD, FBVDDQ



1V8_AON	0.1uF X7R	1uF X6S	4.7uF X6S
N17P	2	1	1
N18P	0	5	3



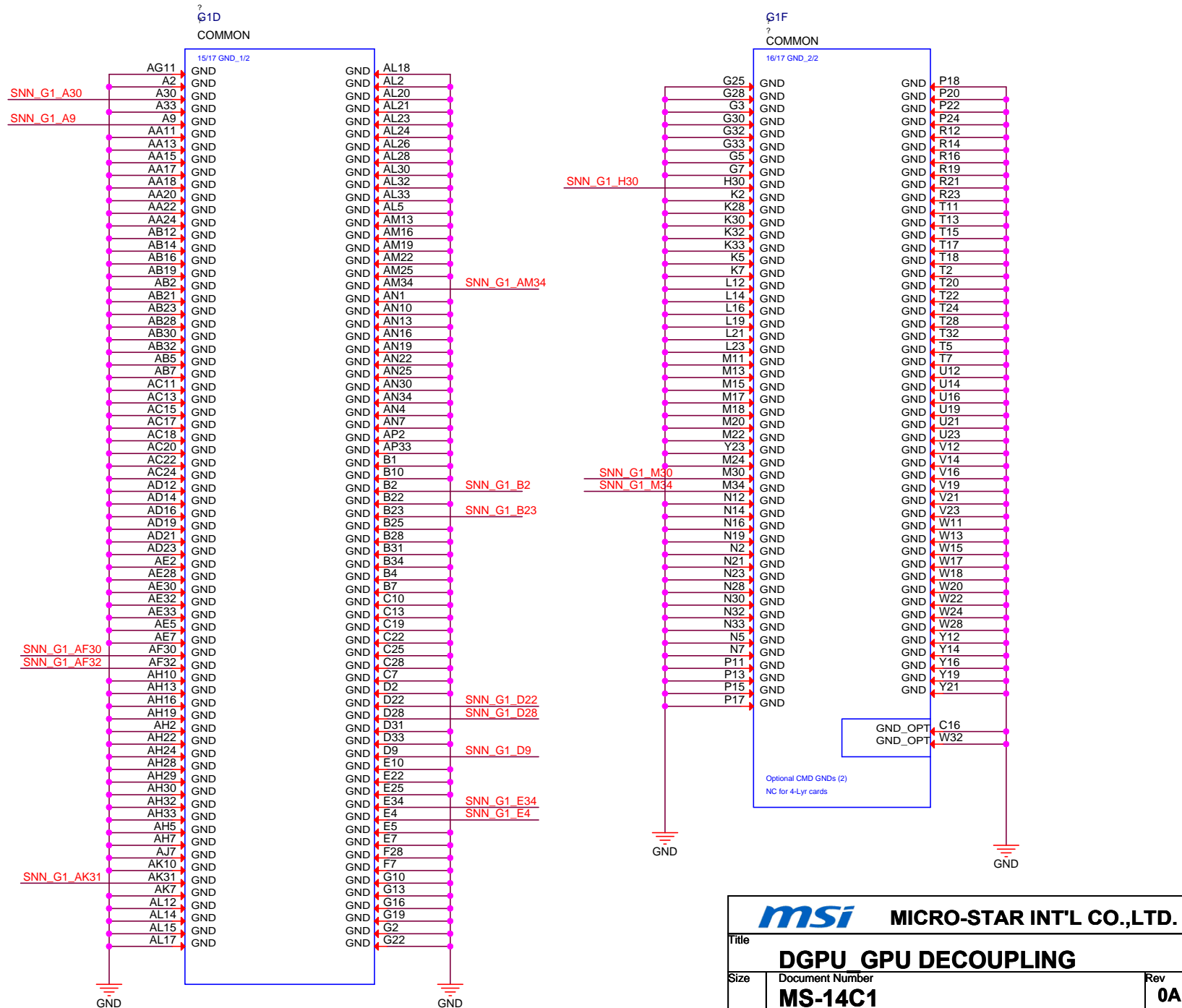
N17P 60.4 OHM	FBCALTERM1 R11-604AT12-W08 X_60.4R1%0402
N18P 40.2 OHM	FBCALTERM2 R11-402AT12-W08 X_40.2R1%0402



FB_CALTERM	
N17P	FB_CALTERM_GND 60.4OHM
N18P	FB_CALTERM_GND 40.2ohm



# DGPU GND



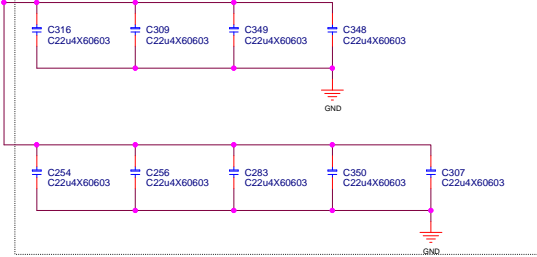


## NVVD

N18P  
330uF x0  
4.7uF x0  
22uF x15  
10uF x 0+34(Under GPU34,Near GPU0)  
0.47uF x26  
1uF x0

N17P  
330uF x1  
4.7uF x2  
22uF x10  
10uF x 11+21(Under GPU21,Near GPU11)  
0.47uF x0  
1uF x13

Place Near to GPU 22uF\*15pcs

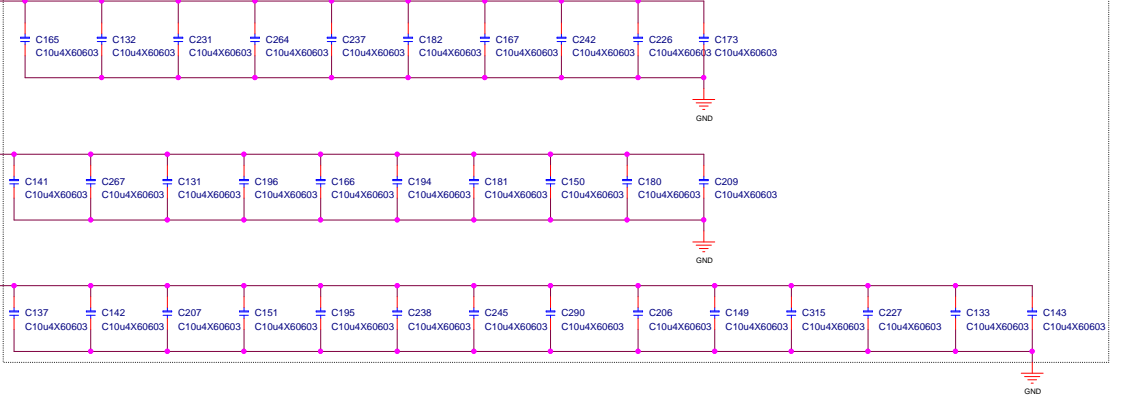


NVVD	1uF X7R	4.7uF X6S	10uF X6S	22uF X6S
N17P	13	2	31	10
N18P	13	0	34	15 9

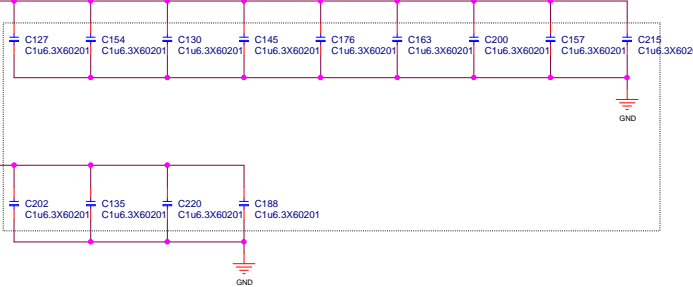
## GPU DECOUPLING

Vinafix.com

Place Under to GPU 10uF\*34pcs



Place under to GPU 18pcs 1u instead of 0.47u N18 :0.47u\*26 change 1u\*13

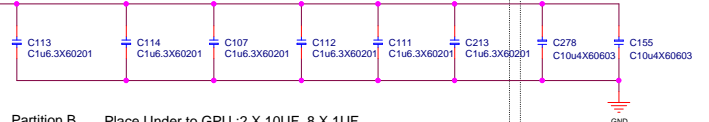


## FBVDDQ

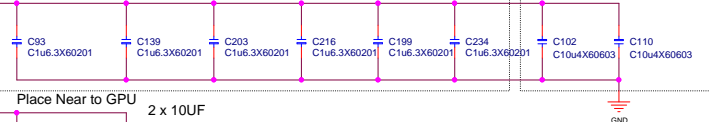
1uF x 16 N18P  
10uF x 6  
22uF x 5

1uF x 12 N17P  
10uF x 6  
22uF x 5

Partition A Place Under to GPU :2 X 10UF, 8 X 1UF N18 :0.47u\*24 change 1u\*12 Under to GPU :10uF\*4



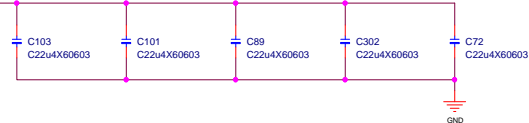
Partition B Place Under to GPU :2 X 10UF, 8 X 1UF



Place Near to GPU 2 x 10UF

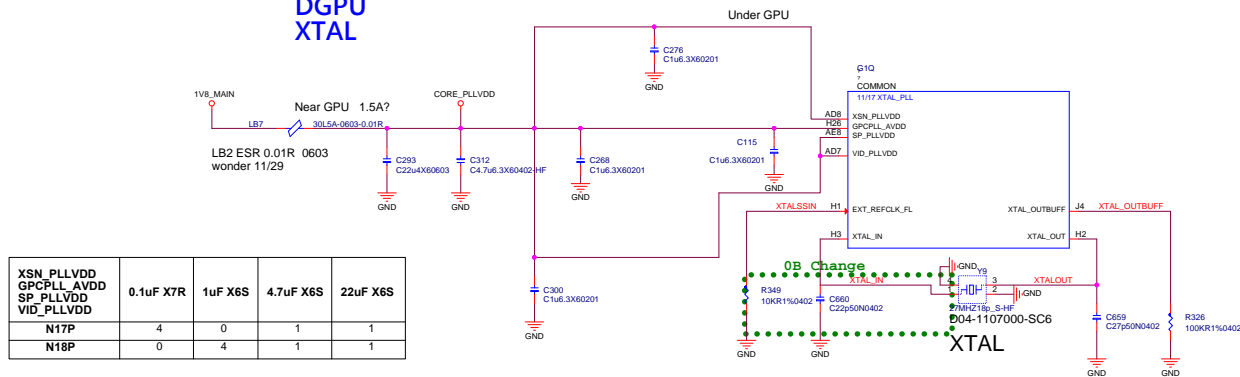
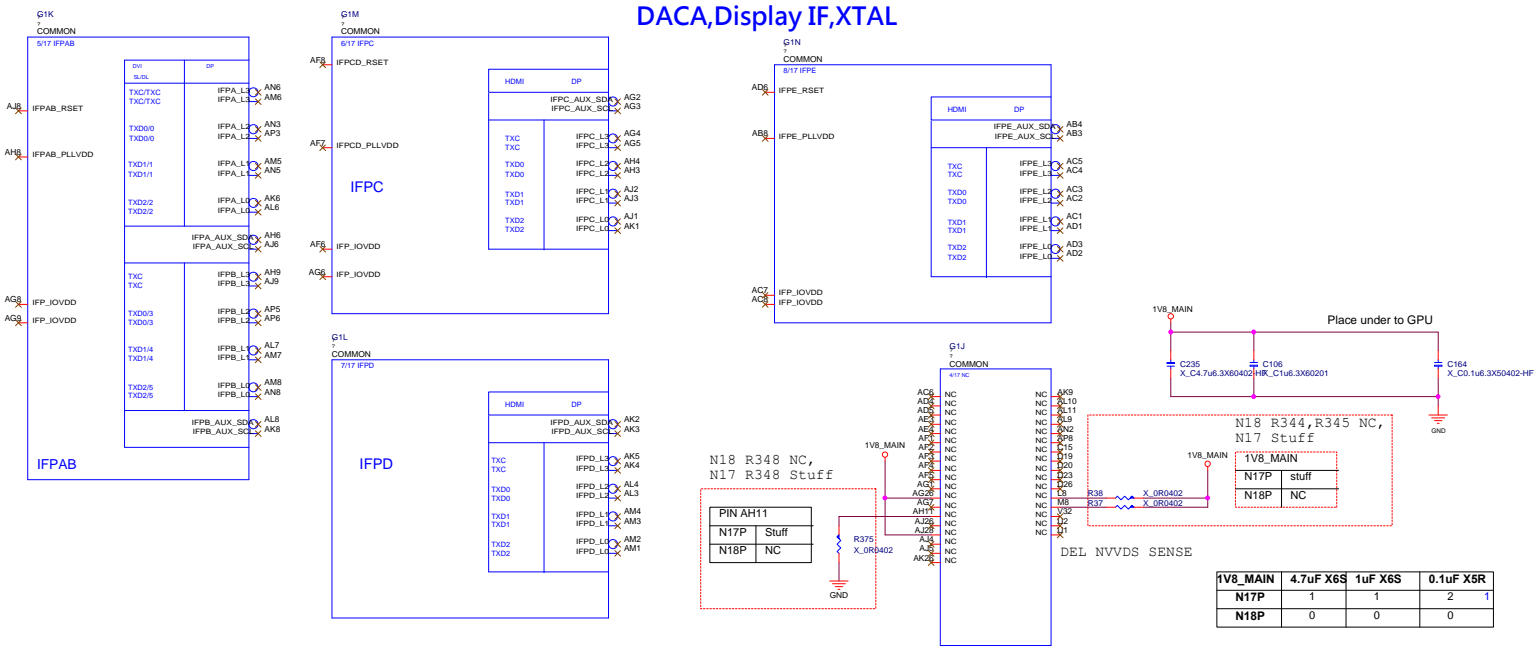


Place Near to GPU 5 x 22UF



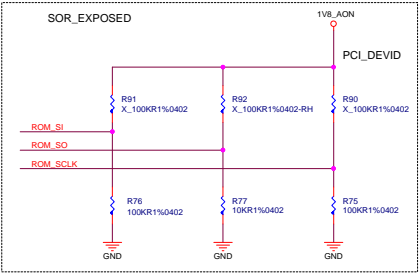
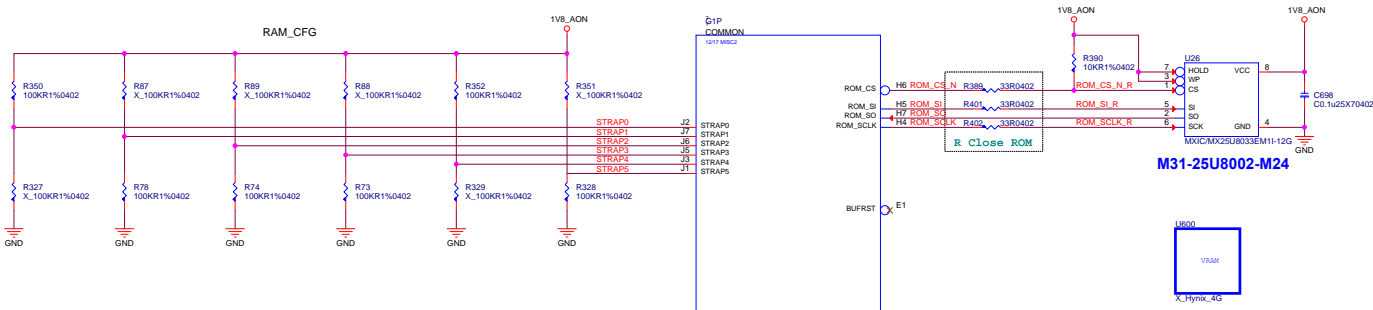
FBVDDQ	1uF X7R	10uF X6S	22uF X6S
N17P	12	6	5
N18P	12	6	5



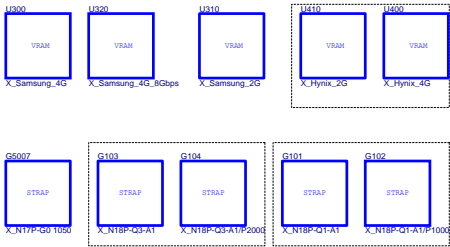




ROM, MULTI-LEVEL STRAPS



8Gbps  
7Gbps



GPU	ROM_SO
N17P	100K
N18P	10K

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE FS_OVERT
H	H	M	0000	V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	L	0	0	0	0

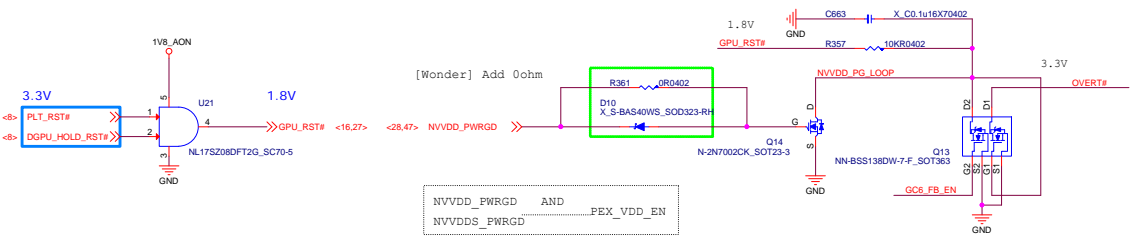
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	STRAP Set
L	L	L	0x0 Samsung: M12-8032545-S02 / K4G80325FB-HC28	4GB R116 R120 R388
L	L	H	0x1 Micron: MT51J256M32HF-70-A	R116 R120 R398
L	H	L	0x2 Hynix: M12-5GC8H05-H23 / H5GC8H24MJR-R0C	4GB R116 R127 R388
L	H	H		
H	L	L		
H	L	H		
H	H	L	0x6 Hynix: M12-5GC4HG5-H23 / H5GC4H24AJR-R0C	2GB R129 R127 R388
H	H	H	0x7 Samsung: M12-41325A5-S02/K4G41325FE-HC28	2GB R129 R127 R398
L	L	M	0x8 Micron: EDW032BAG-70-F-A	R116 R120 R398/R388
L	M	L		

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	STRAP Set
L	L	L	0x0 Samsung: K4G80325FC-HC25 :C	4GB R116 R120 R388
L	L	H	0x1 Micron: MT51J256M32HF-80:B	4GB R116 R120 R398
L	H	L	0x2 Hynix: H5GC8H24AJR-R2C :A	4GB R116 R127 R388

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE  
  
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V





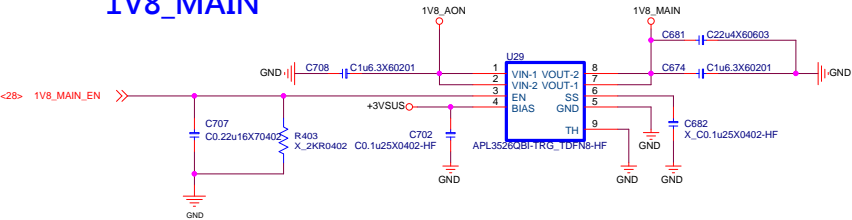


NVIDIA Power Sequence Control

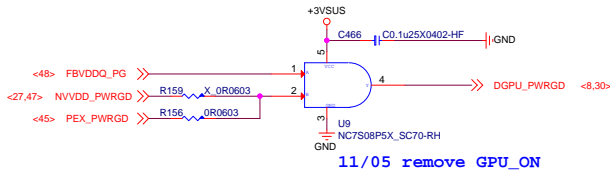
Power on = 1V8\_AON -> 1V8\_MAIN -> 3V3\_NV/NVDD -> NVDDS/PEX\_VDD -> FBVDDQ -> DGPUPWRGD

Power down = NVDDS -> PEX\_VDD -> NVVDD/FBVDDQ -> 3V3\_NV -> 1V8\_MAIN -> 1V8\_AON

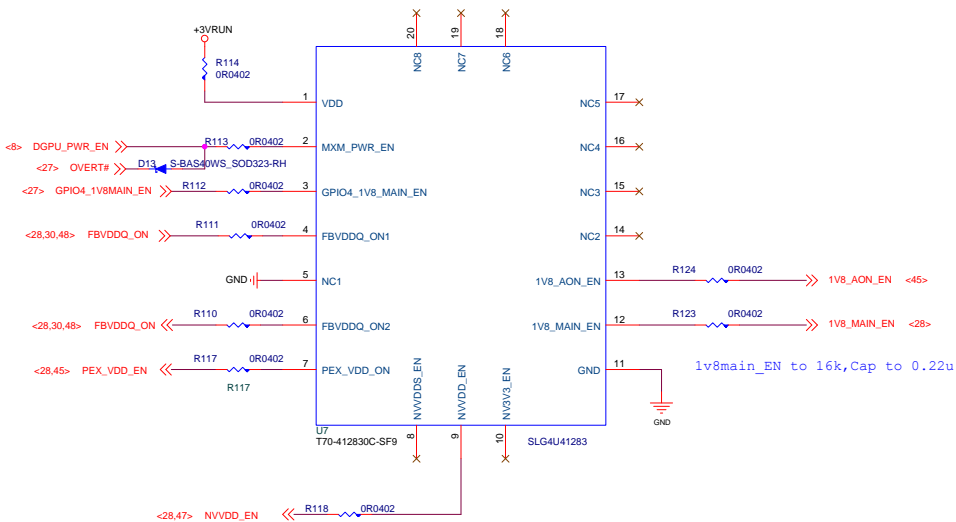
1V8\_MAIN



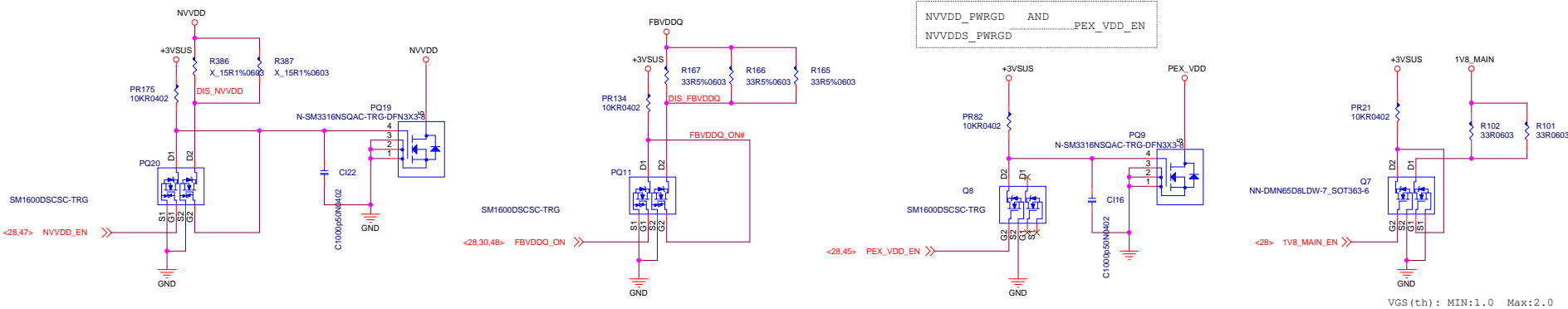
DGPU POWER GOOD



SLG4U41283 power sequence control IC



Discharge





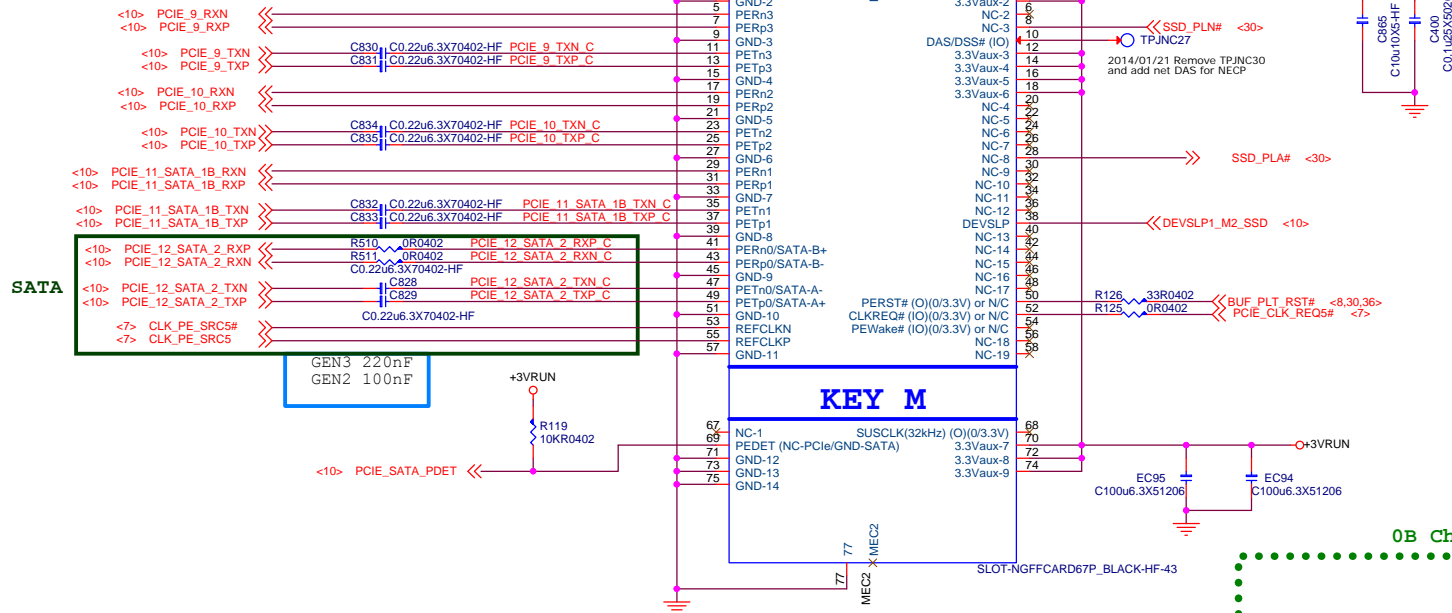




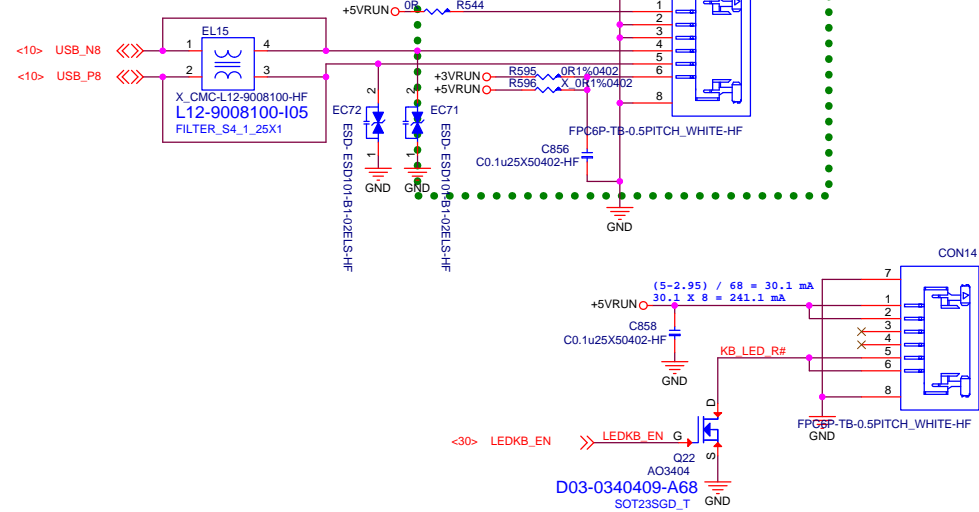
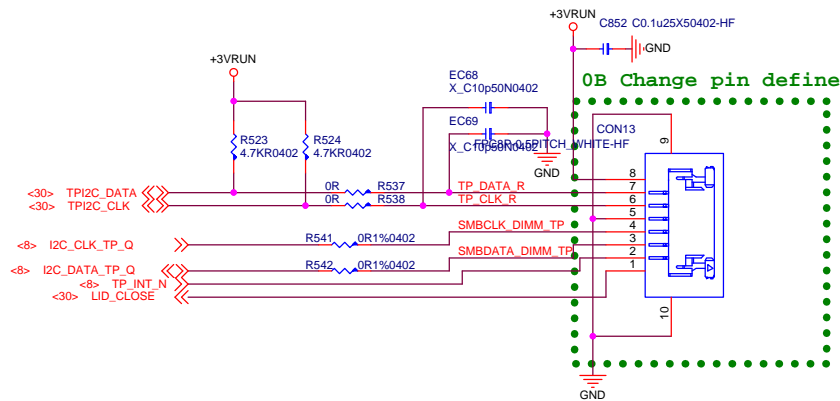




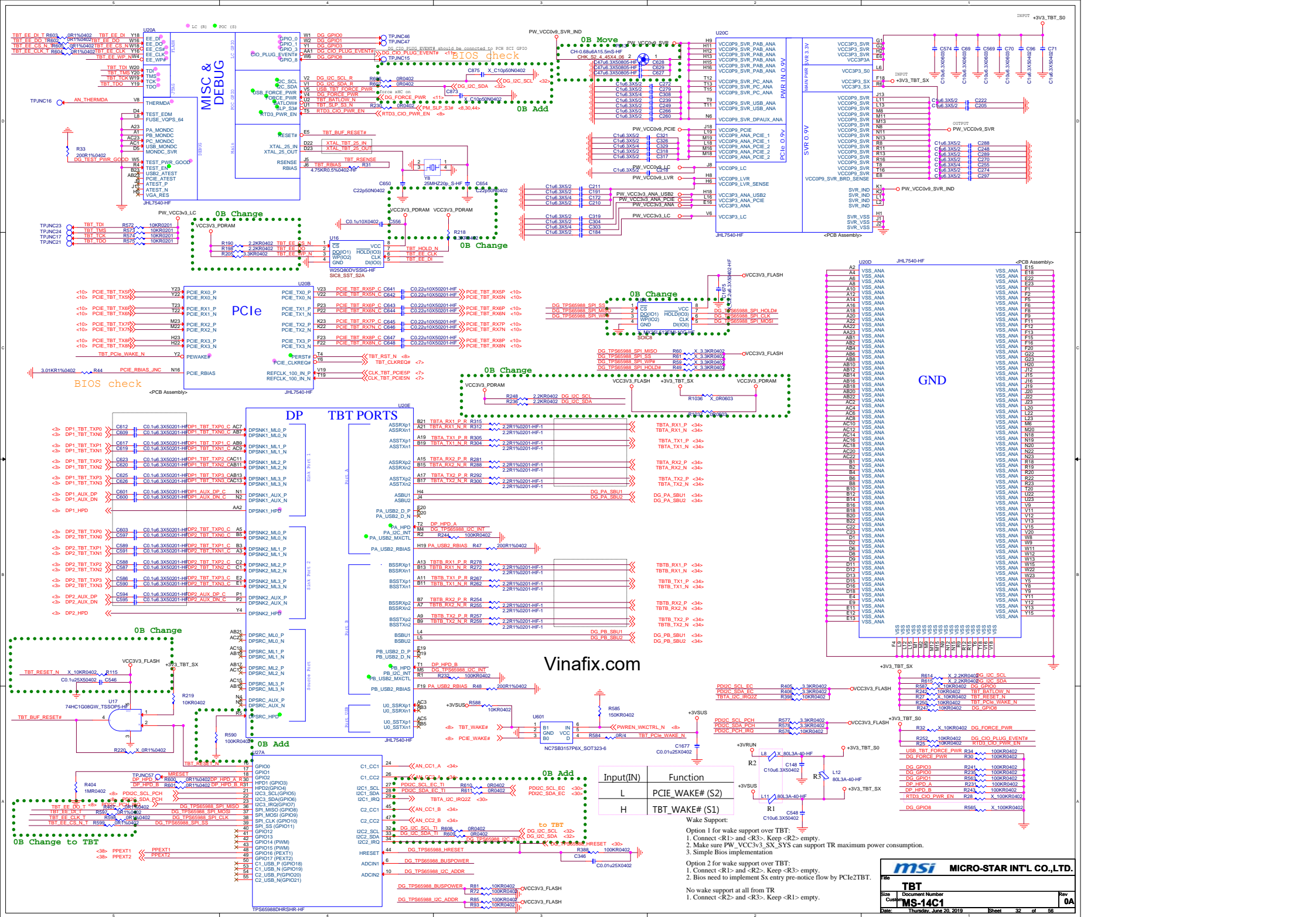
# PCIEx4 /SATA Reversal SSD



Click Pad







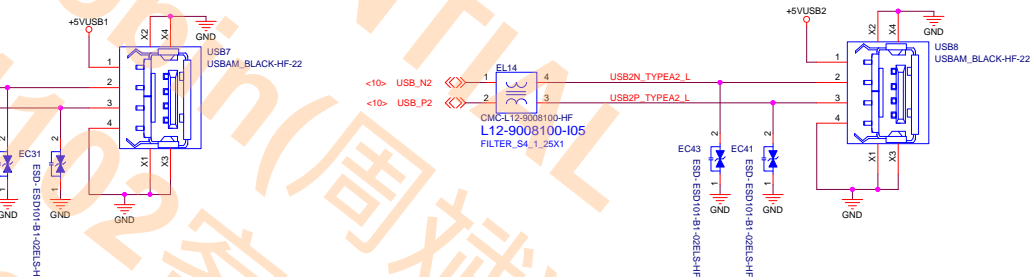
Vinafix.com

Input(IN)	Function
L	PCIE_WAKE# (S2)
H	TBT_WAKE# (S1)

Wake Support:

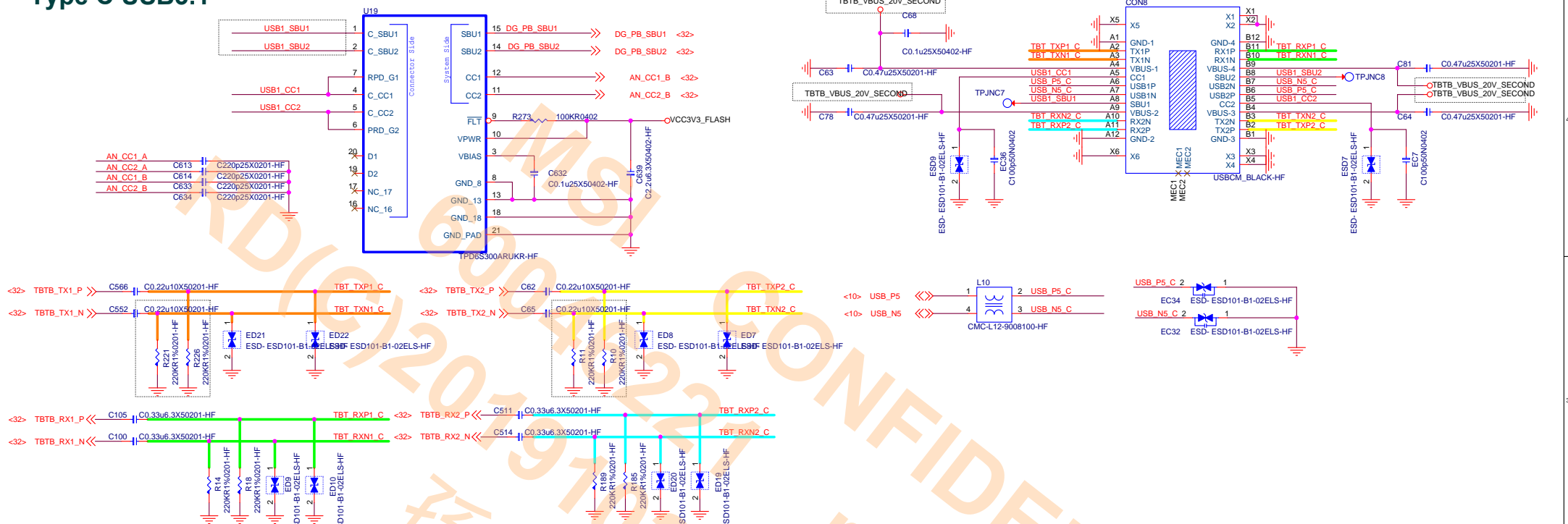
- Option 1 for wake support over TBT:
1. Connect <R1> and <R3>. Keep <R2> empty.
  2. Make sure PW\_VCC3V3\_SX\_SYS can support TR maximum power consumption.
  3. Simple Bios implementation
- Option 2 for wake support over TBT:
1. Connect <R1> and <R2>. Keep <R3> empty.
  2. Bios need to implement Sx entry pre-notice flow by PCIe2TBT.
- No wake support at all from TR
1. Connect <R2> and <R3>. Keep <R1> empty.



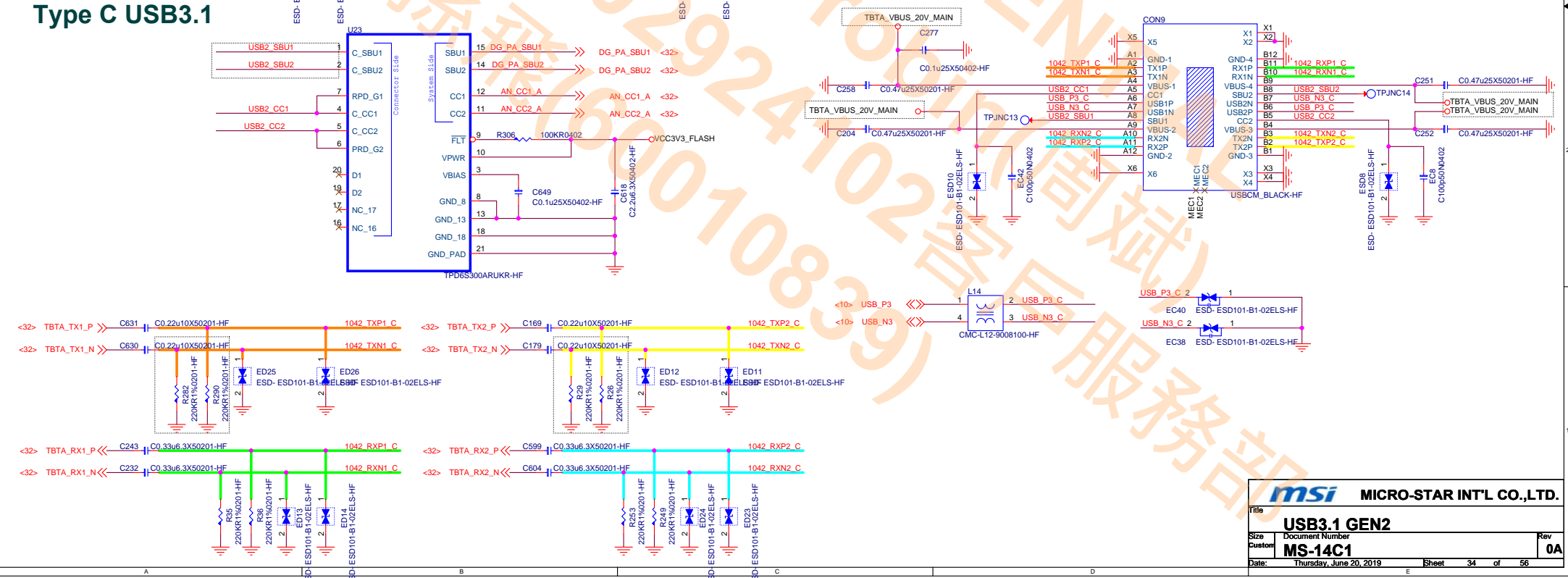




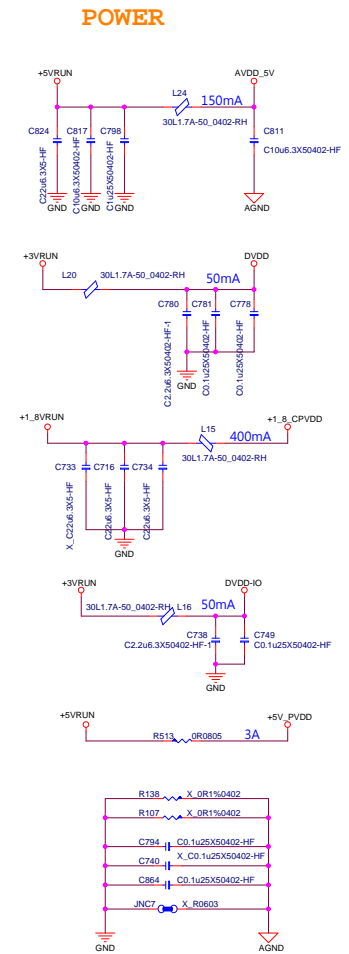
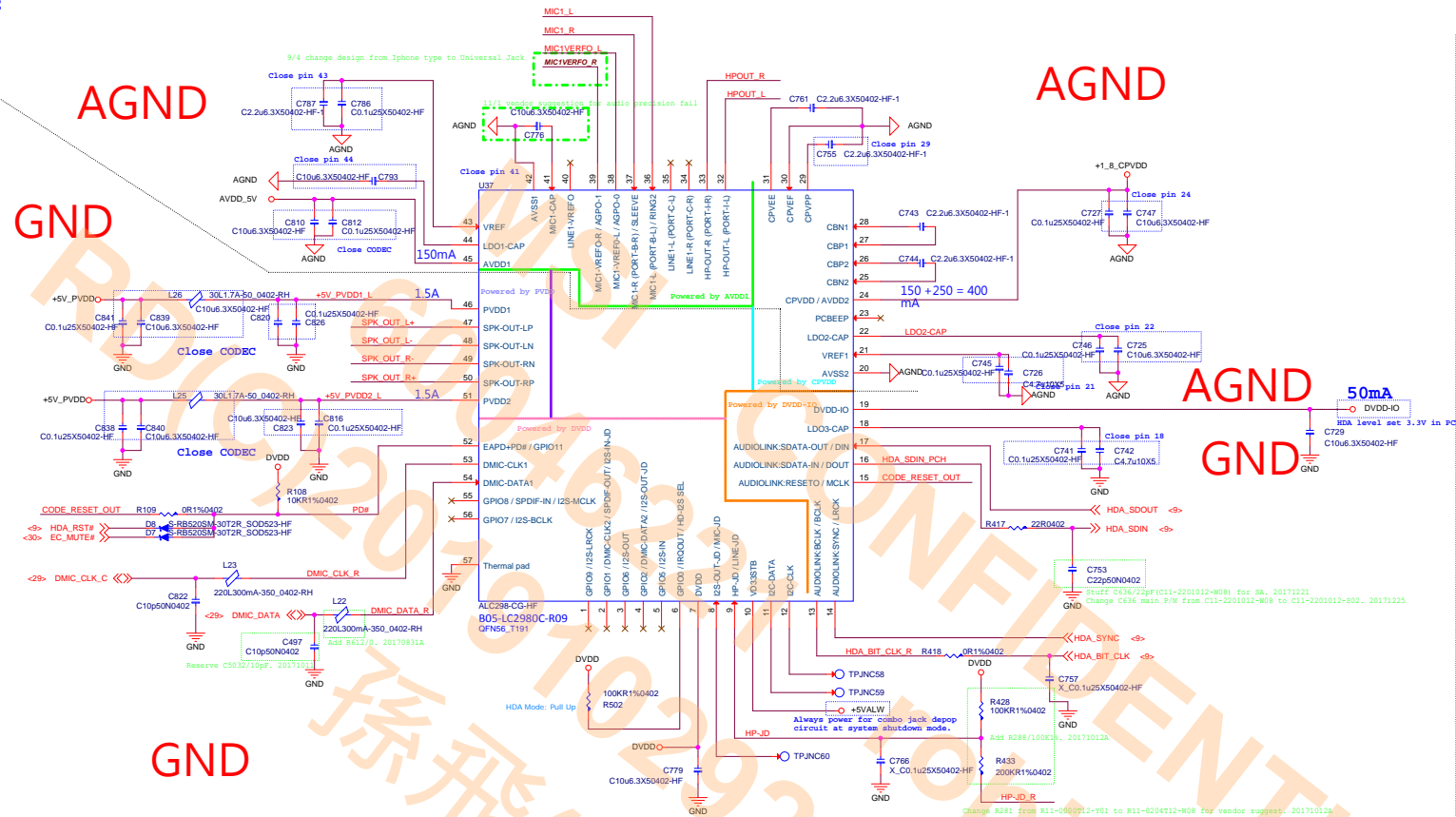
# Type C USB3.1



# Type C USB3.1



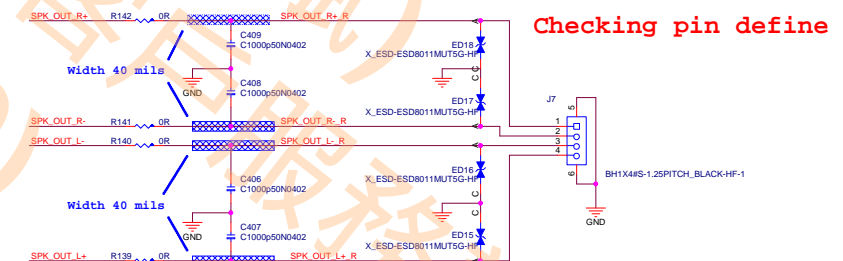




## SPEAKER

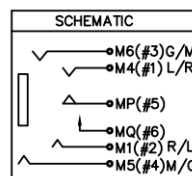
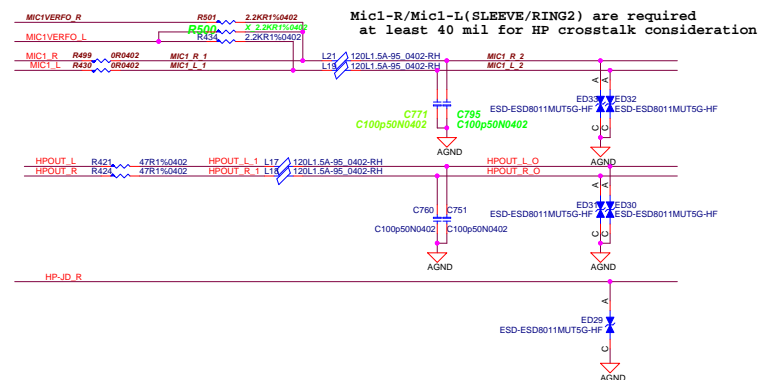
- 1.SP.K L+ L- R+ R- trace width: Speaker 4 ohm ==> 40 mils  
Speaker 8 ohm ==> 20 mils
- 2.If you mount the LC filter(L1-L4,C4/C11,C2/C7/C10/C13),Please let them together and close to codec.
- 3.Please make the trace length/ Speaker wire length of SP.K L+/L-/R+/R- be the same as possible as you can.
- 4.If L1,L2,L3,L4 are replaced by 0 ohm/1.6A resistor,please don't use general bead, because it may influence the THD+N quality, and C4,C11 should be NC

## Checking pin define



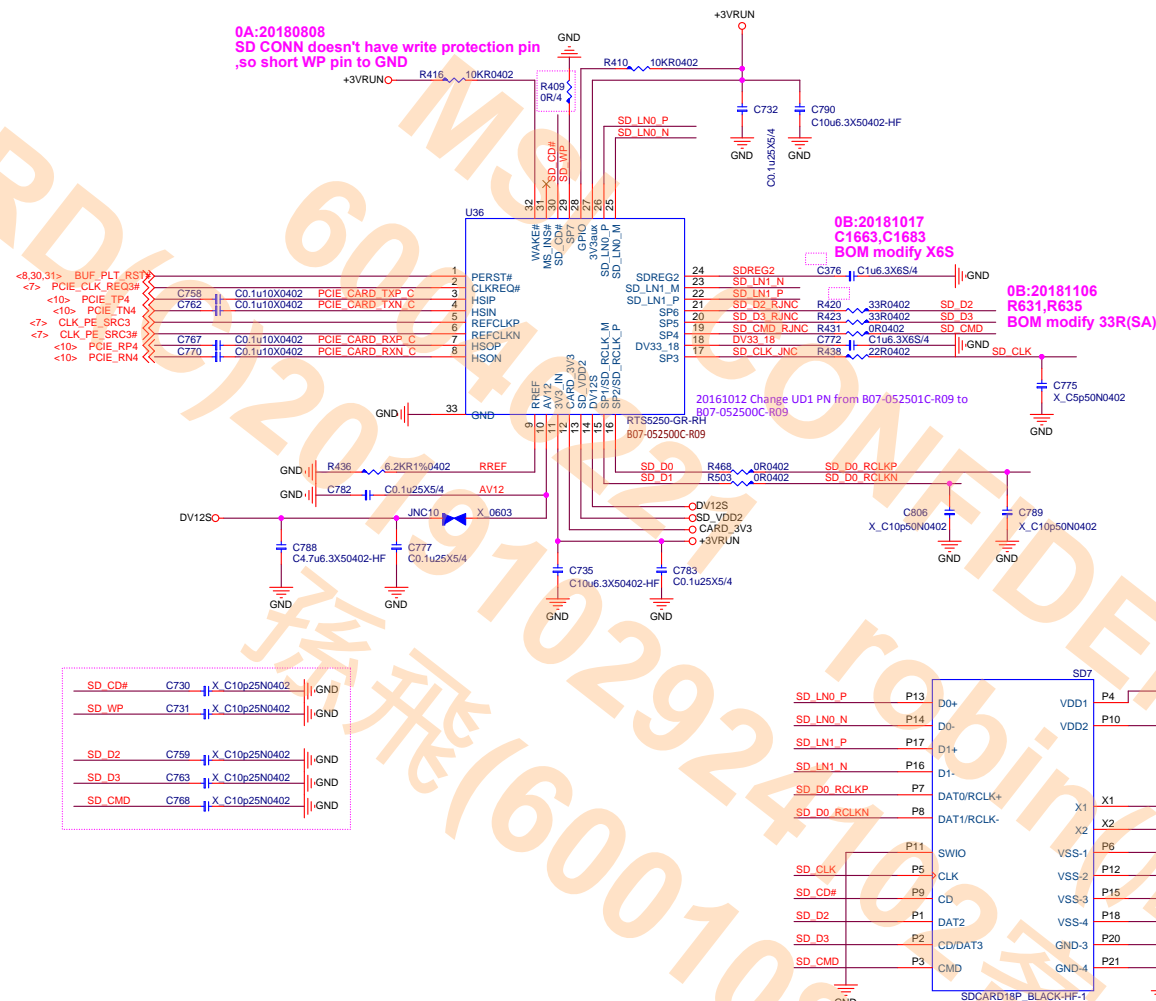
## Universal Jack


9/4 change design from Iphone type to Universal Jack





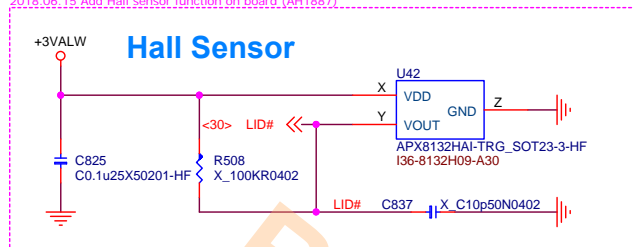
## CardReader ( RTS5250 )



 <b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b> <b>Card Reader(RTS5250)</b>	
<b>Size</b> <b>Custom</b>	<b>Document Number</b> <b>MS-14C1</b>
<b>Date:</b> Friday, June 21, 2019	<b>Sheet</b> 36 <b>of</b> 56
<b>Rev</b> <b>0A</b>	

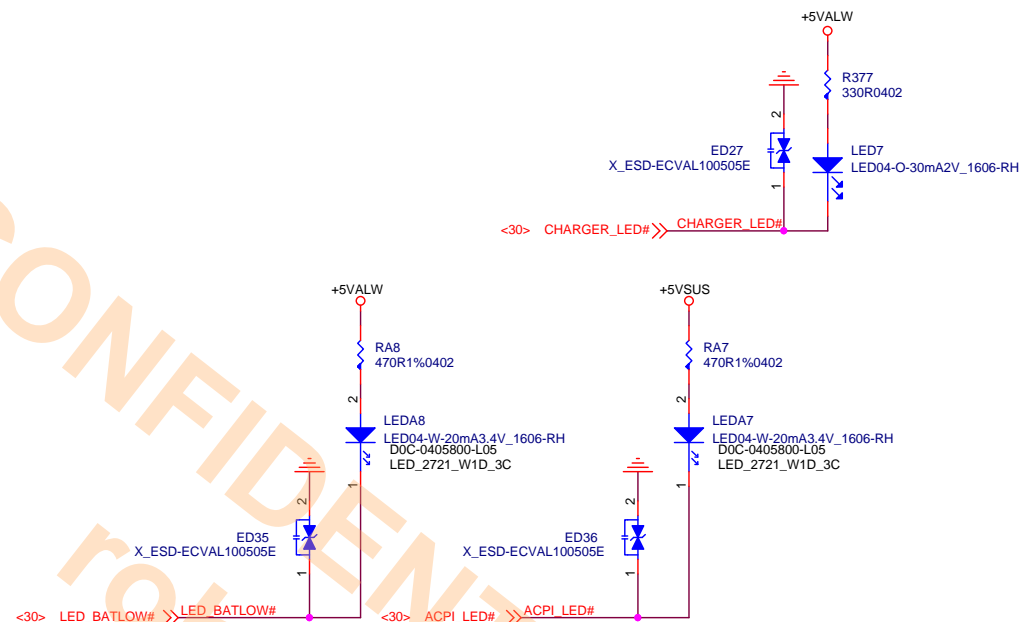


2018.06.20 Change hall sensor IC from AH1887 (2 output) to AH1810 (1 output)  
2018.06.15 Add Hall sensor function on board (AH1887)



2018.06.26 Change hall sensor IC from AH1810 to APX8132 by ME suggest

## LED



**msi**

MICRO-STAR INT'L CO.,LTD.

Title

**PWR SW/FP/LED/LID**

Size  
Custom

Document Number

**MS-14C1**

Rev

**0A**

Date:

Thursday, June 20, 2019

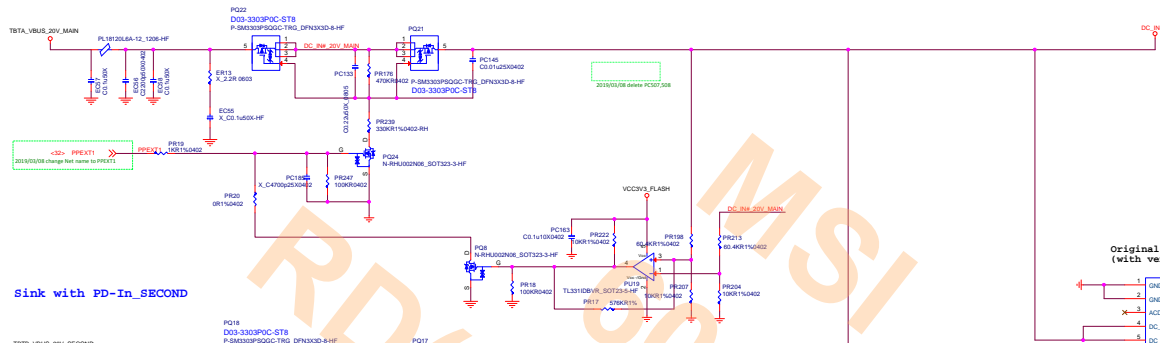
Sheet

37 of 56

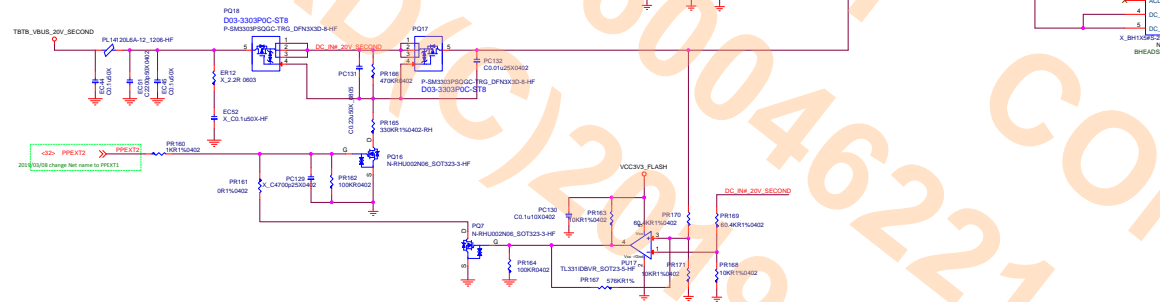
E



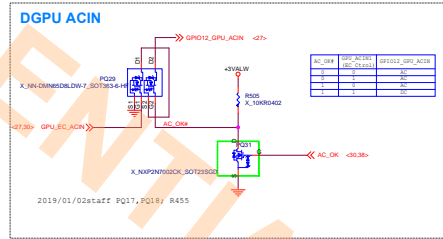
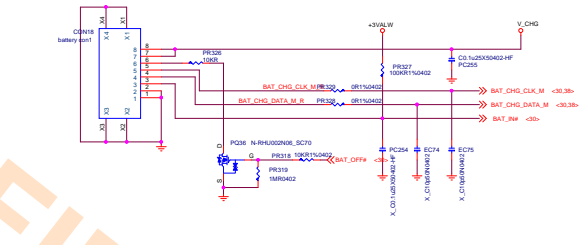
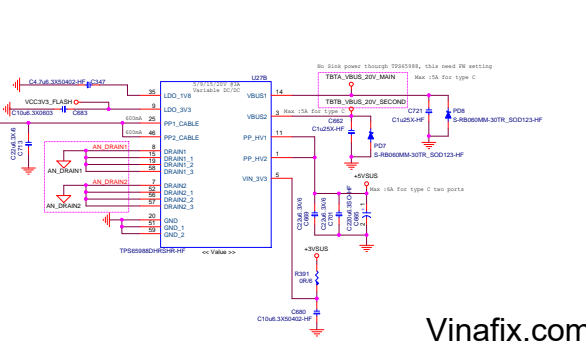
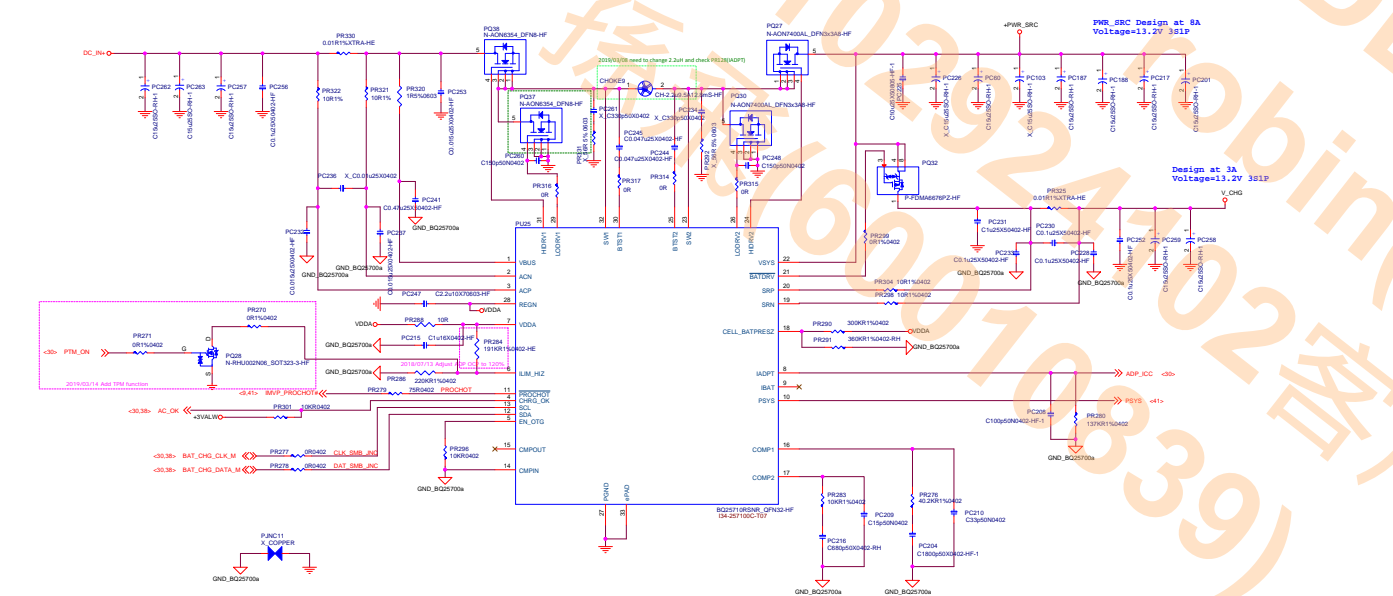
# Sink with PD-In\_MAIN



# Sink with PD-In\_SECOND



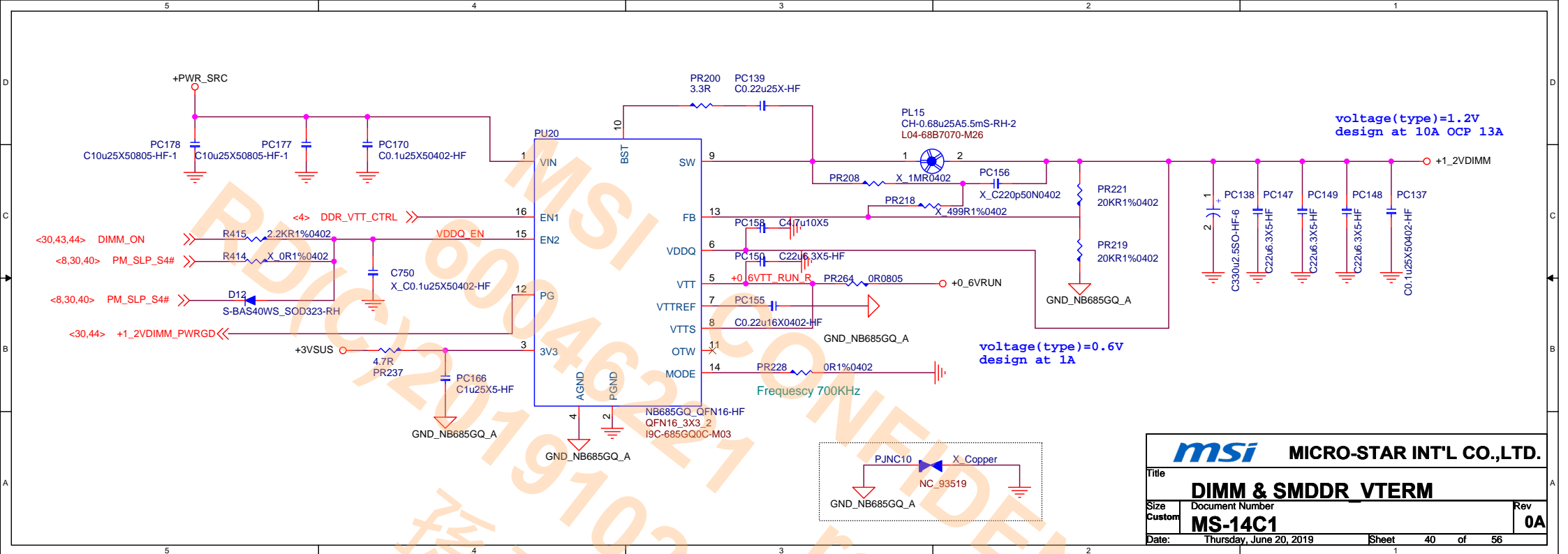
# Battery Charger







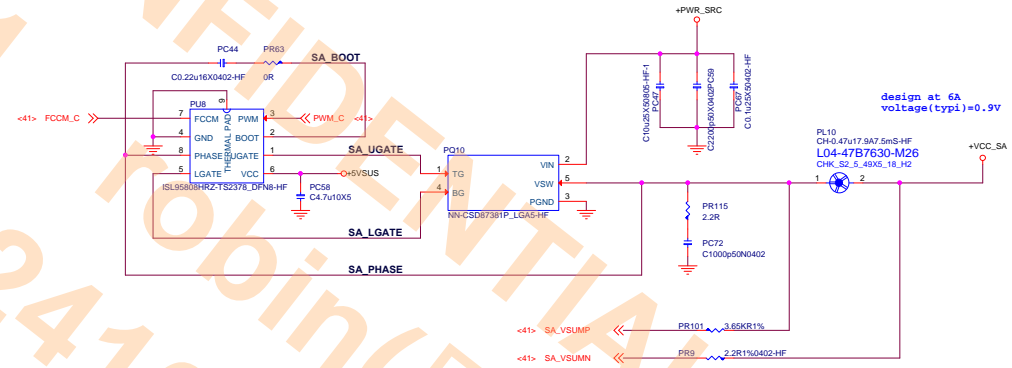
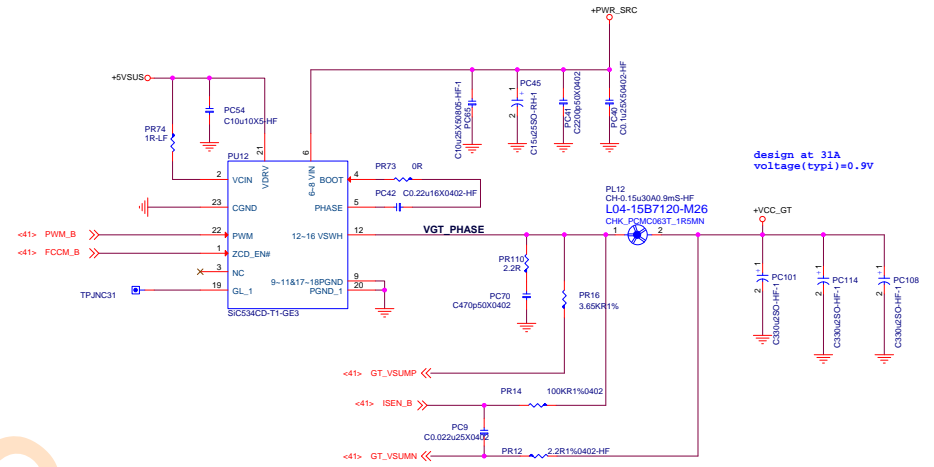








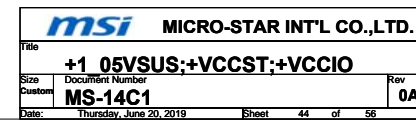
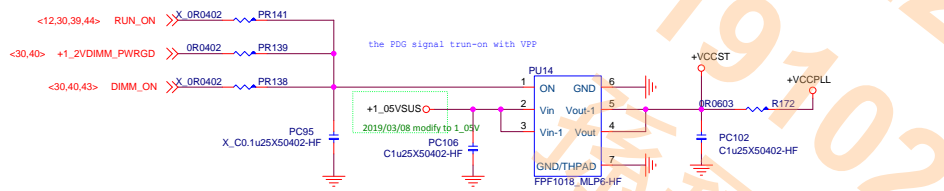
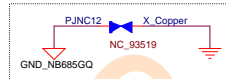


[illegible]







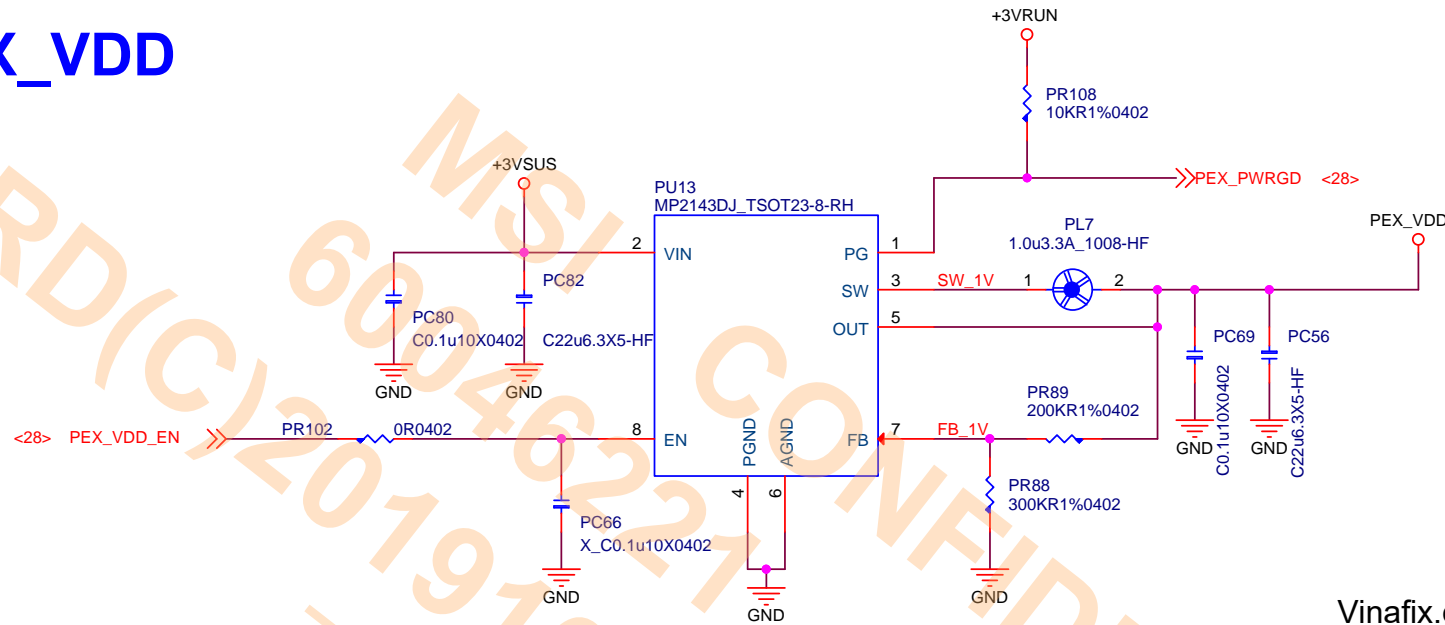




# PEX\_VDD

## PEX\_VDD

Voltage = 1.0V  
Current = 1.6A  
OCP(typi) = 4.8A

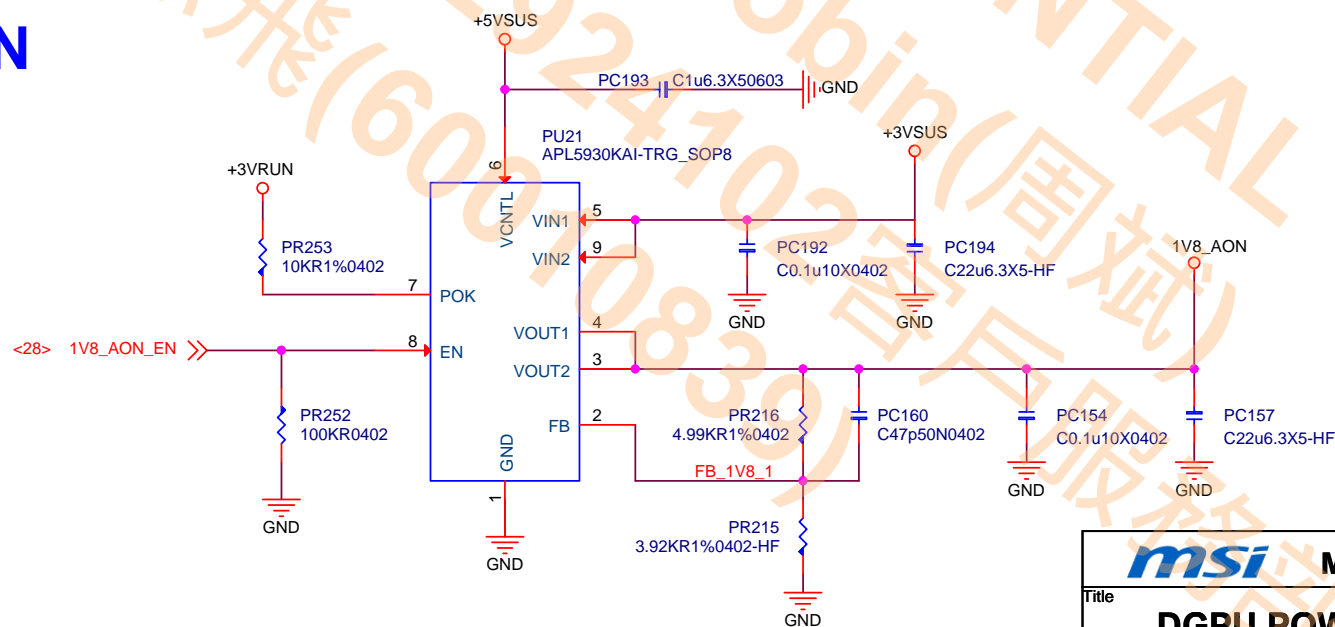


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# 1V8\_AON

## 1V8\_AON

Voltage = 1.8V  
Current = 2.3A



**msi**

**MICRO-STAR INT'L CO.,LTD.**

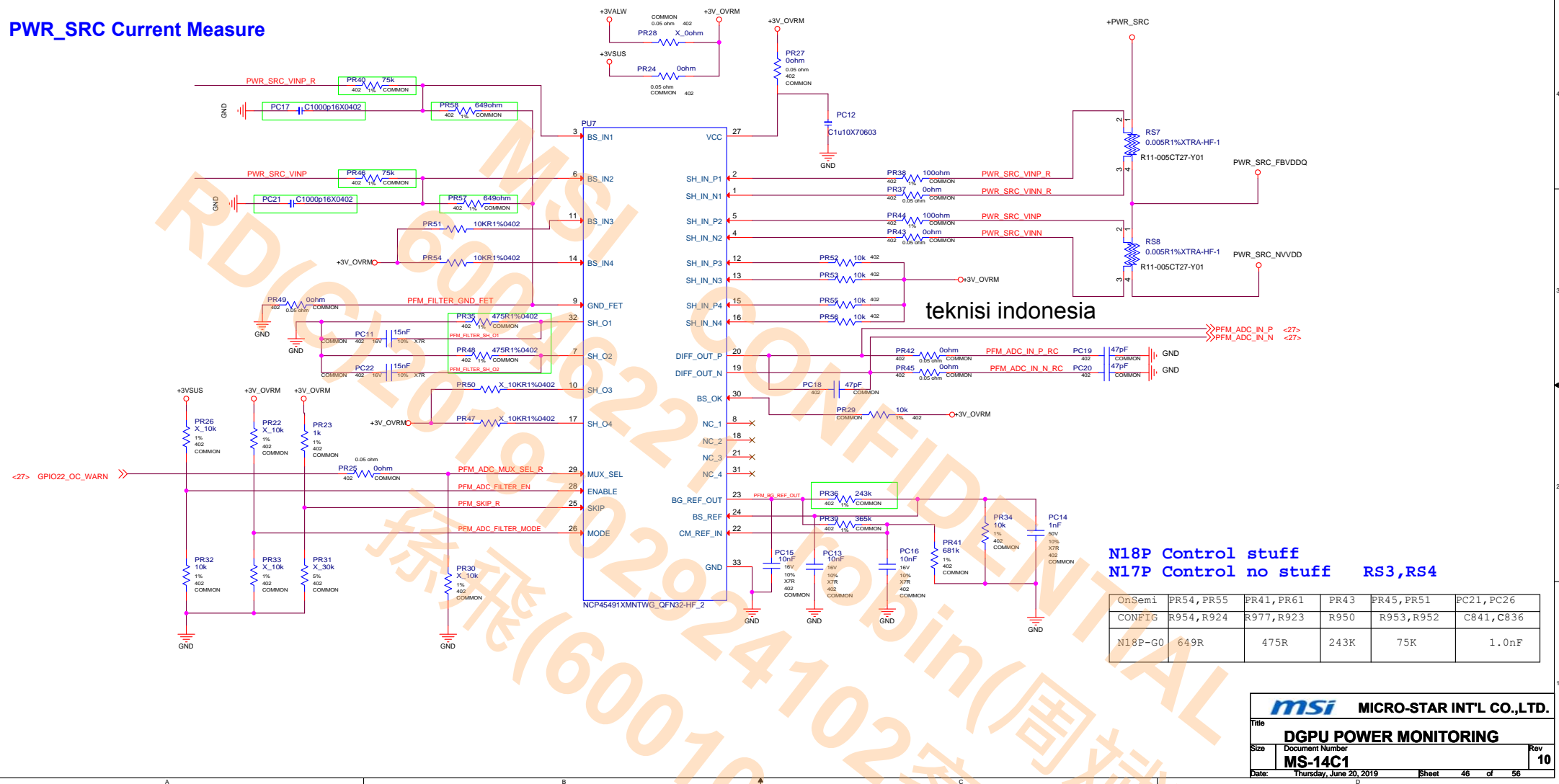
Title **DGPU POWER PEX\_VDD/1V8\_AON**

Size Custom Document Number **MS-14C1** Rev **0A**

Date: Thursday, June 20, 2019 Sheet 45 of 56

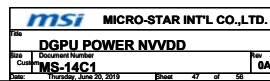


# PWR\_SRC Current Measure





**EDP-Peak 150A**  
**EDP-Con 35A for N18P-G0 MAX-Q**

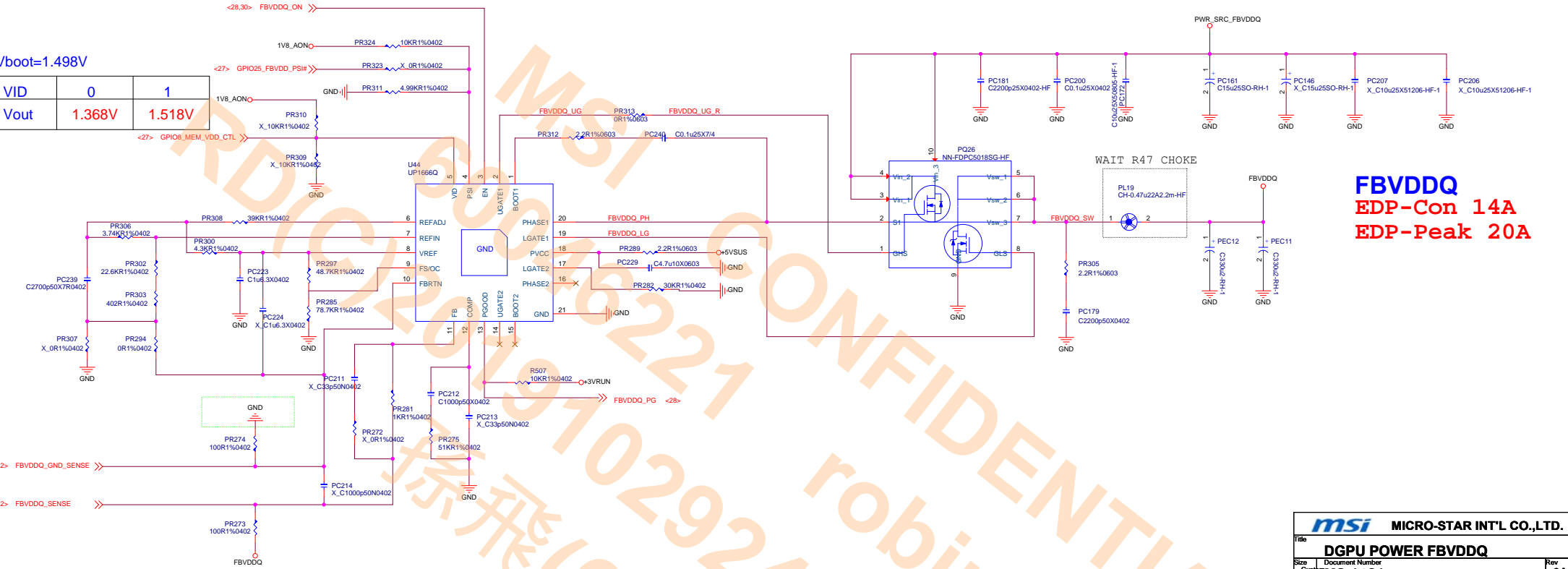




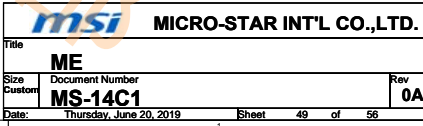
FBVDDQ

Vboot=1.498V

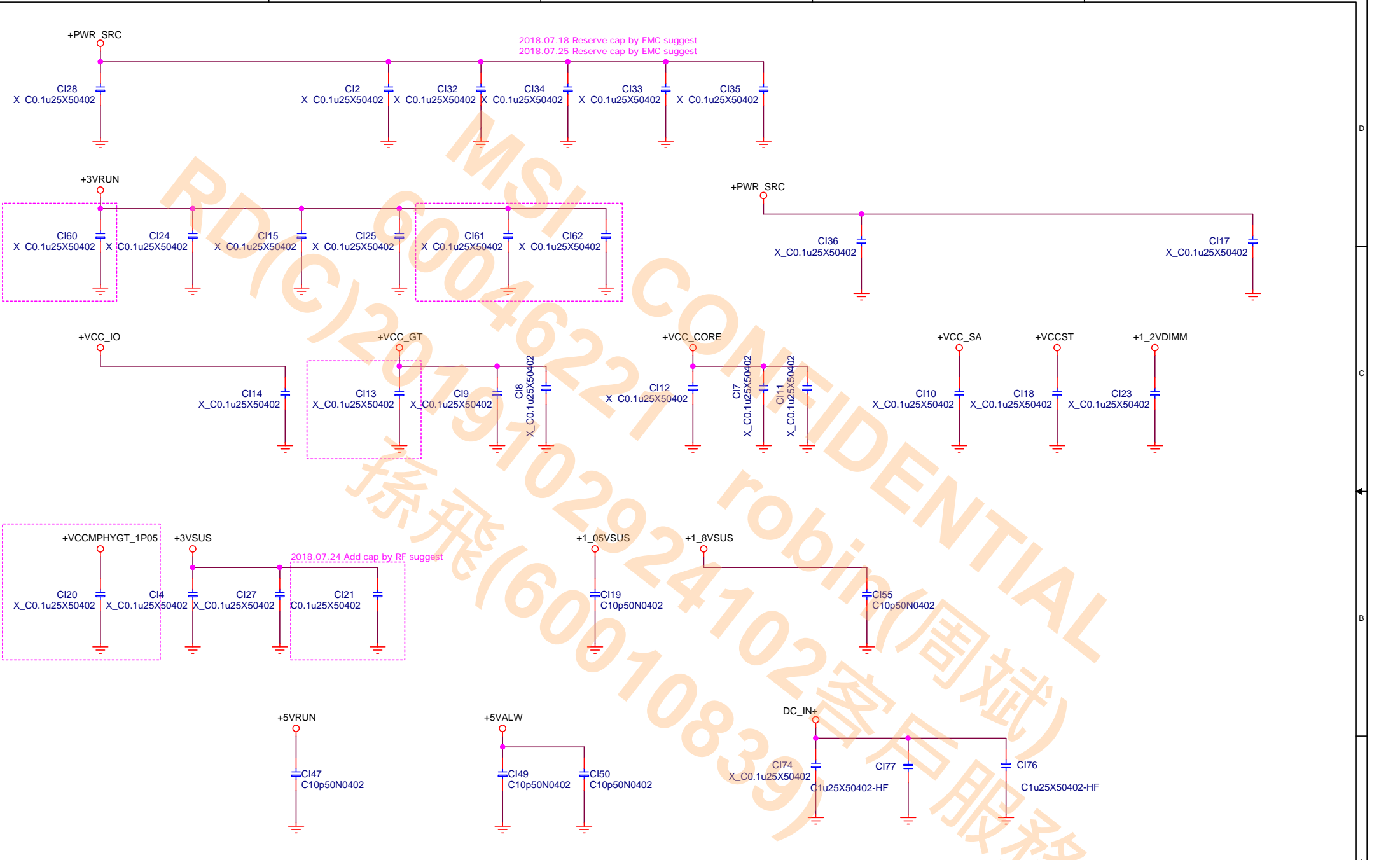
VID	0	1
Vout	1.368V	1.518V



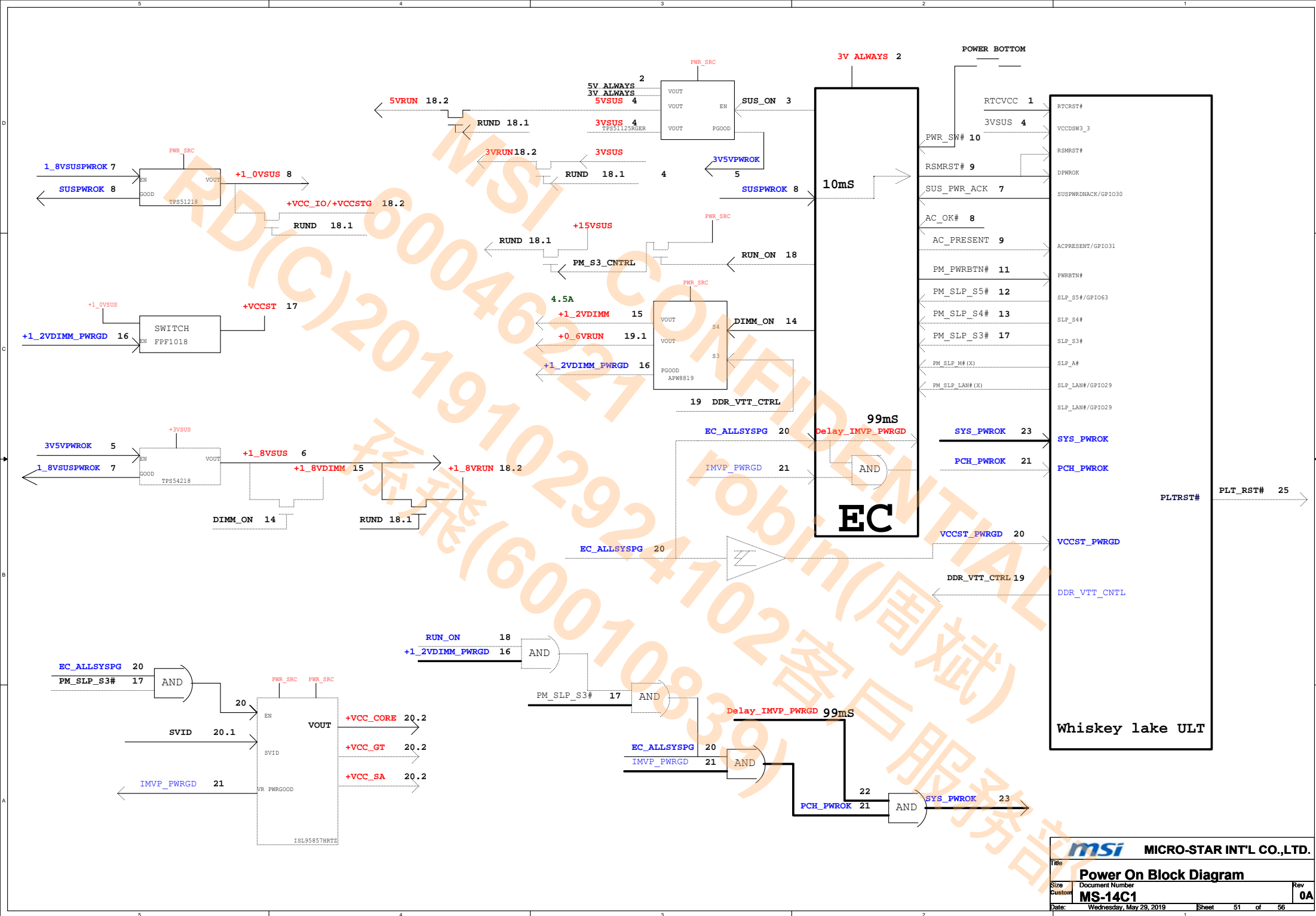






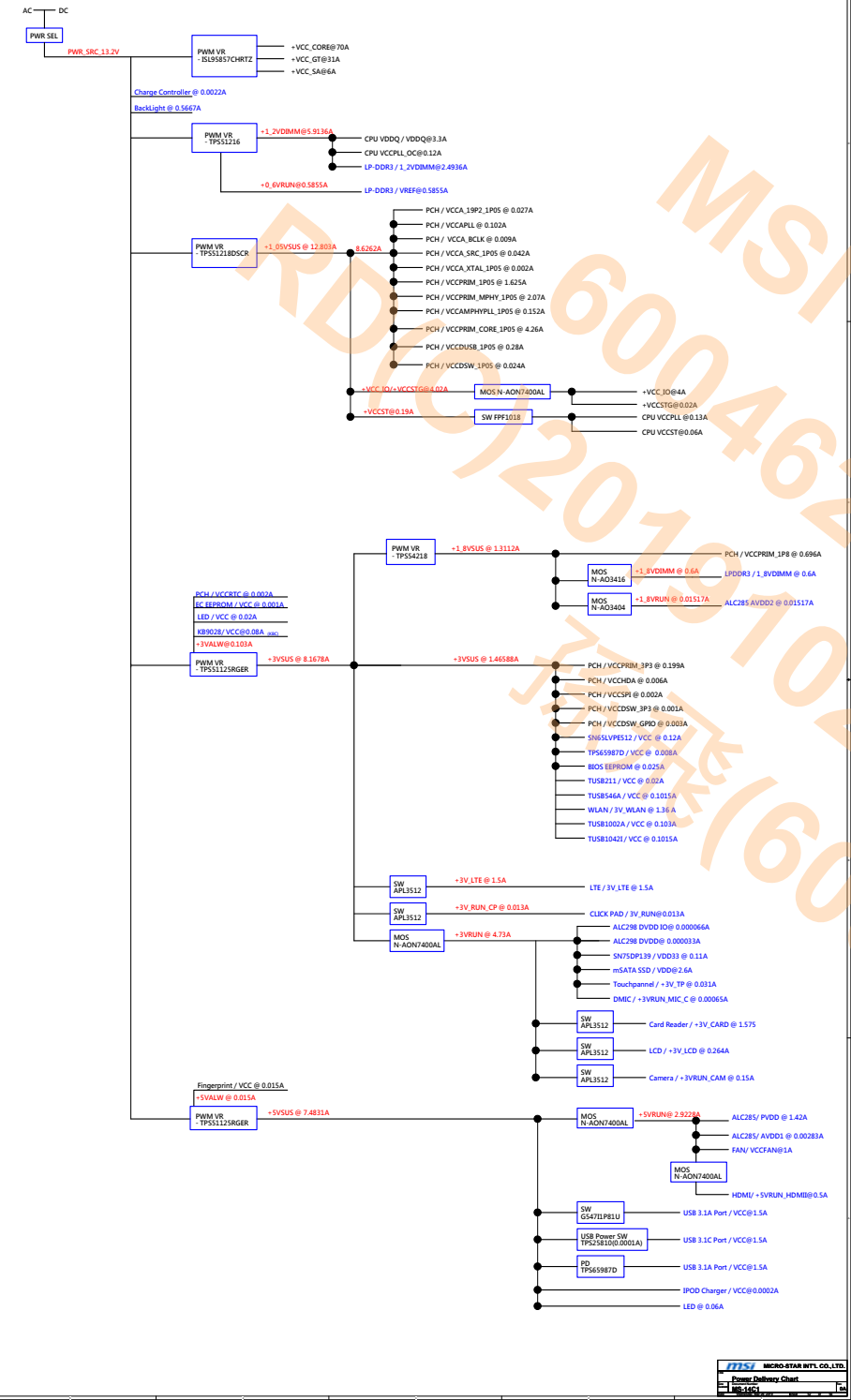








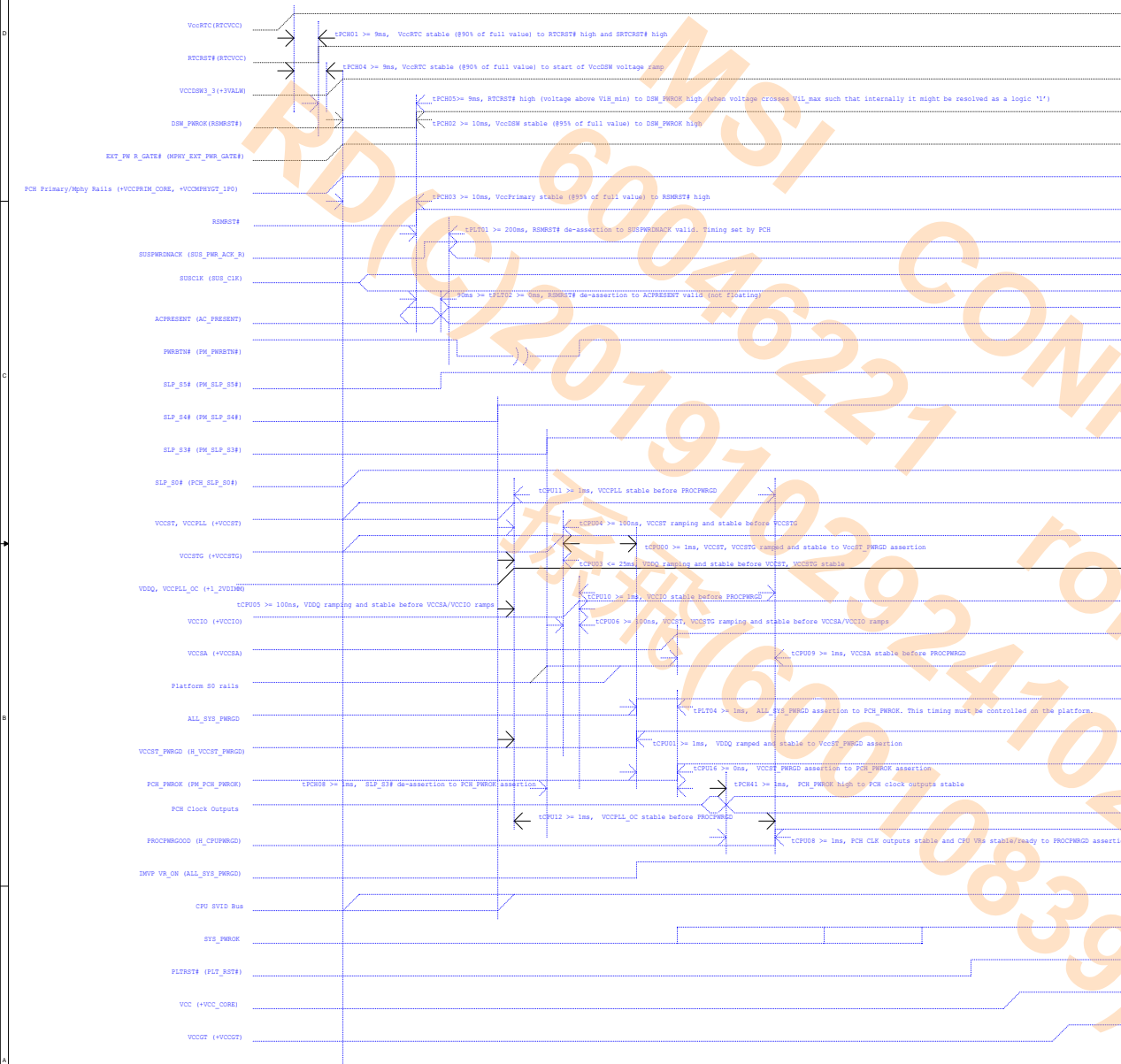
13H1 Power Delivery Chart



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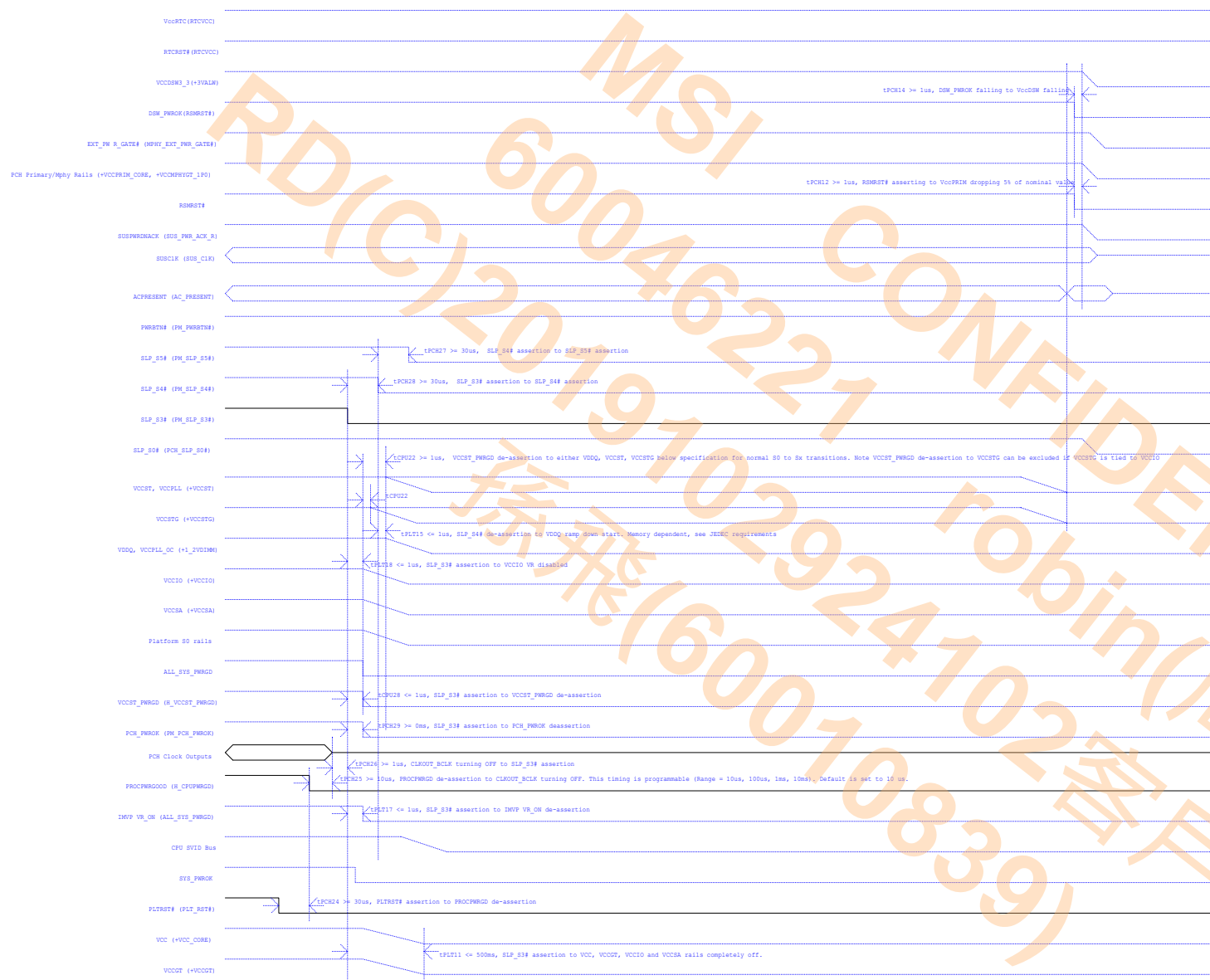


# G3 to S0





# S0 to G3





497: 2018/11/02 Page18 Add R485 for TP525B10 overcurrent heat issue  
498: 2018/11/02 Page18 Add Type-C\_OCR of signal for TP525B10 overcurrent heat issue (Shut TP5WC173)  
499: 2018/11/02 Page11 Change signal from USB\_OC# to Type-C\_OC# for TP525B10 overcurrent heat issue  
500: 2018/11/06 Page18 Update PCB shielding symbol by manufacturing suggest  
501: 2018/11/06 Page11 Un-stuff R213 because IC control pin is push-out by NEC request  
502: 2018/11/13 Page18 Change C261 from 220uf to 470uf for SA request  
503: 2018/11/13 Page11 Change R213 R174 from 0 ohm to 100 ohm by NEC request  
504: 2018/11/16 Page22 Change F2011 F2012 from AC20802 to AC20806 for USB 3.0 bus leak by NEC request  
505: 2018/11/16 Page25 Det F2014 F2016 and add ED109 ED110 ED111 ED112 From ES08040 to F208015M for PS-component add by NEC request  
506: 2018/11/16 Page18 Change R433 from 100 ohm to 500 ohm by NEC request  
507: 2018/11/16 Page25 Change R422 from 243 ohm to 390 ohm by NEC request  
508: 2018/11/19 Page20 Remove L1M633 by ME request  
509: 2018/11/19 Page24 Change R17 value from 2.2kOhm to 10kOhm for ME cannot be detected  
510: 2018/11/22 Page18 Det RTC crystal 2nd source, Remove RTC crystal virtual component(176)  
511: 2018/11/22 Page18 Add virtual component for JSM crystal by different ROM(177)  
512: 2018/11/22 Page17 Shift EC115,EC116,EC18,EC19 by EM suggest  
513: 2018/11/27 Page27 Change C418 from 100uf to 220uf for voltage drop of +5V\_LTE  
514: 2018/11/29 Page18 Change ME voltage(L1M630) main source from 50V-50V12V1\_GND to 50V-50V12V1\_R62 by ME request  
515: 2018/11/29 Page24 Change T10A1002A setting for vendor suggest(CH2\_C02\_C02\_002 from 1.0 to R\_R6)  
516: 2018/11/29 Page18 Add WiFi Module Adapter by ME request (L1M630)  
517: 2018/11/29 Page25 Add Power Adapter Type 2 by ME request (L1M631)  
518: 2018/11/29 Page18 Add Power Adapter Type 2 by ME request (L1M631)  
519: 2018/11/29 Page18 Add Router (Square) by ME request (L1M631)  
520: 2018/11/29 Page18 Add Router (Square) by ME request (L1M631)  
521: 2018/11/29 Page18 Add Router (Circle) by ME request (L1M631)  
522: 2018/11/29 Page18 Add SMA Connector Adapter by ME request (L1M630)  
523: 2018/11/29 Page18 Change PCB 974 from P03-1301120-H71 to P03-1301120-H73 (PCB2)  
524: 2018/11/19 Page23 Un-stuff R515 for Type-C USB 3.1 GEN2 compliance test by NEC request  
525: 2018/11/16 Page23 Change R225 R123 from 20K ohm to 1K ohm for Type-A compliance test by NEC request  
526: 2018/11/17 Page18 L1M670 and L1M671 change to Un-stuff by ME request  
527: 2018/12/17 Page18 Add Thermal CONR Sponge for S063 by ME request (L1M637)

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孫飛(60010839) 客戶服務部



